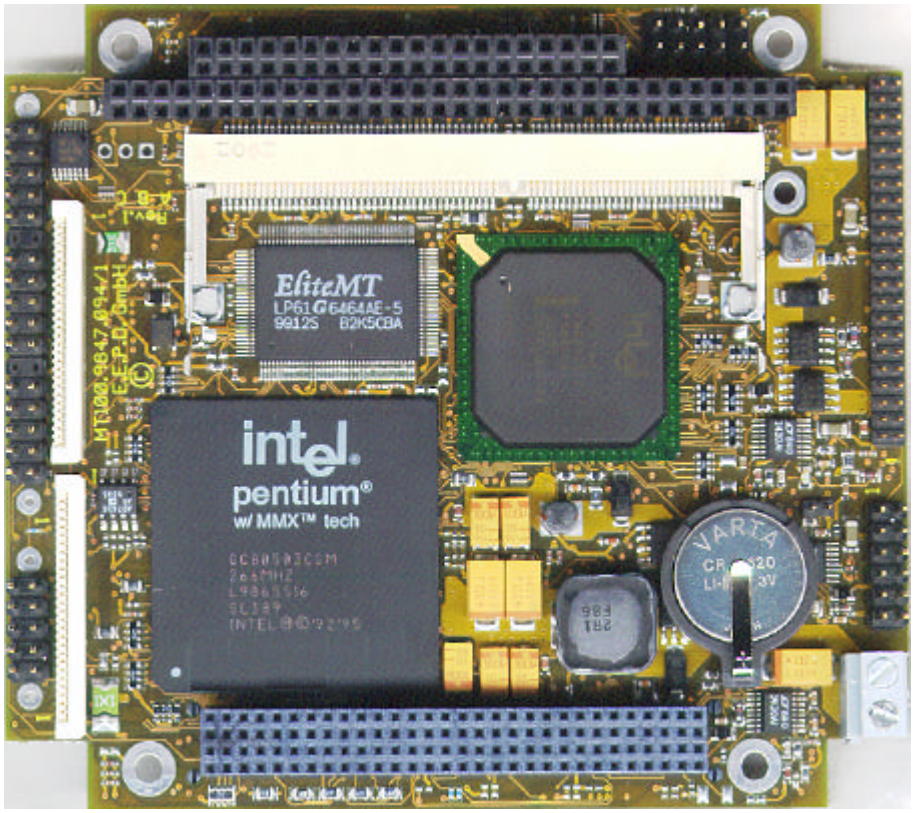
profive

CPU-T5

USER-MANUAL



PC104-*Plus* PROFIVE®-CPU-T5 Motherboard Rev 2
with Intel Pentium MMX 166/266 MHz

this document covers CPU-T5 Rev. 2 or higher

a product "Made in Germany"

by

E.E.P.D. Electronic Equipment
Produktion & Distribution GmbH

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1 General Notes

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- This product cannot be used as a stand alone product!
- Therefore it has to be integrated together with other products like power-supplies, graphic-boards etc. to be functional.
- To meet FCC and CE requirements every component as well as the combination of all components have to be validated against all standards required for the end-product.
- In order to meet FCC and CE requirements this product has to be integrated into a proper housing which provides appropriate shielding and insulation.
- It is on the customers sole responsibility to assure that his end-product meets all required standards.
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This product will be free from defects in workmanship and material under normal and proper use for 18 months after date of the original shipment.

In the event of a warranty claim for defects which appear within the warranty period, customer shall deliver the product along with proof of purchase to the original place of purchase, shipping prepaid. Repair, replacement or refund of the purchase price of the defective product will be at the sole option of the manufacturer. All transportation risks and costs in connection with warranty service are the responsibility of the customer.

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2 History

Date	Version	Changes
May 11th , 1999	1.0	Initial release
July 8th , 1999	1.1	Polarity of Backup Battery changed (CPU-T5 Rev 2)
August 9th, 1999	1.2	Pinout Description COM1,2,3,4 corrected
October 14th, 1999	1.3	Product Description modified, LPT Pinout
March 15th,2000	1.4	Capters 6 (BIOS) added, Chapter 7 (Utility Software) updated, Software Manual added, WDT-Demo Code added
March 27th, 2000	1.5	Factory defaults of VCC_MESS min and VCC_MESS max have changed

3 Unpacking Instruction

Please check that your card contains below mentioned items.
If something is damaged, missing or if your PROFIVE® CPU-T5 board is not inside the original packaging, please inform the forwarder and your supplier at once, otherwise your claims cannot be accepted.

First you should read all instructions and kindly note all said informations before connecting any cable to the PROFIVE CPU-T5 card.
Only by doing so the function and the quality of this product can be guaranteed.

The following components should have come with the PROFIVE CPU-T5 board
PROFIVE CPU-T5 card with
1 x CD-ROM with utility-software, user manual (PDF-file)
1 x Lithium battery for real time clock backup
1 x Bag with mounting screws, nuts and bolts
Different cable sets and a starter-kit are optionally available, see appendix for details.

4 Product Description

4.1 General Technical Description

- Complete PC-compatible motherboard with INTEL® Pentium™ MMX with either 166 MHz or 266 MHz CPU (0.25µ Technology)
- Intel 440 TX Chipset

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- 512 kB second level cache
- DIMM-SO II Module EDO/SDRAM up to 128 MB
- Flash System BIOS
- Voltage, temperature and fan monitor
- Optional Compact-Flash Adapter up to 128 MB
- Low Power Consumption: typical 5W (166 MHz) / 8W (266 MHz)
- Single supply: +5 V DC ±5%
- Dual USB on board
- Four RS 232 serial ports (up to 115.200 baud) ESD-protected[1]
- 32-bit-PCI-Bus with a bus-clock-frequency of 33 MHz
- 16-bit-ISA-Bus with a bus-clock-frequency of 8,25MHz
- External speaker connector
- Optional fan connector
- Size of the card: 111 mm x 96 mm (PC/104-*Plus* size including allowed connector size)
- Max. operating temperature: 0°C to 60°C ambient or 0°C to 70°C at any point on the modules surface, with adequate airflow
- Max. storage temperature: -20°C to +100°C
- Max. rel. Humidity of atmosphere non condensing: working 80% / storage 95%
- SMD-technology is used to ensure high quality, reliability and an optimum price/performance ratio
- 10-layer-PCB with micro-via-technology
- Made in Germany
- PC/104 compatible (ISA-Bus)
- PC/104-*Plus* compatible (PCI-Bus)
- Ruggedized versions available (contact E.E.P.D. GmbH for further informations)

[1] Complies with 89/336/EEC EMC Directive
ESD Protection to IEC1000-4-2 (801.2)
± 8 kV: Contact Discharge
±15 kV: Air-Gap Discharge
±15 kV: Human Body Model

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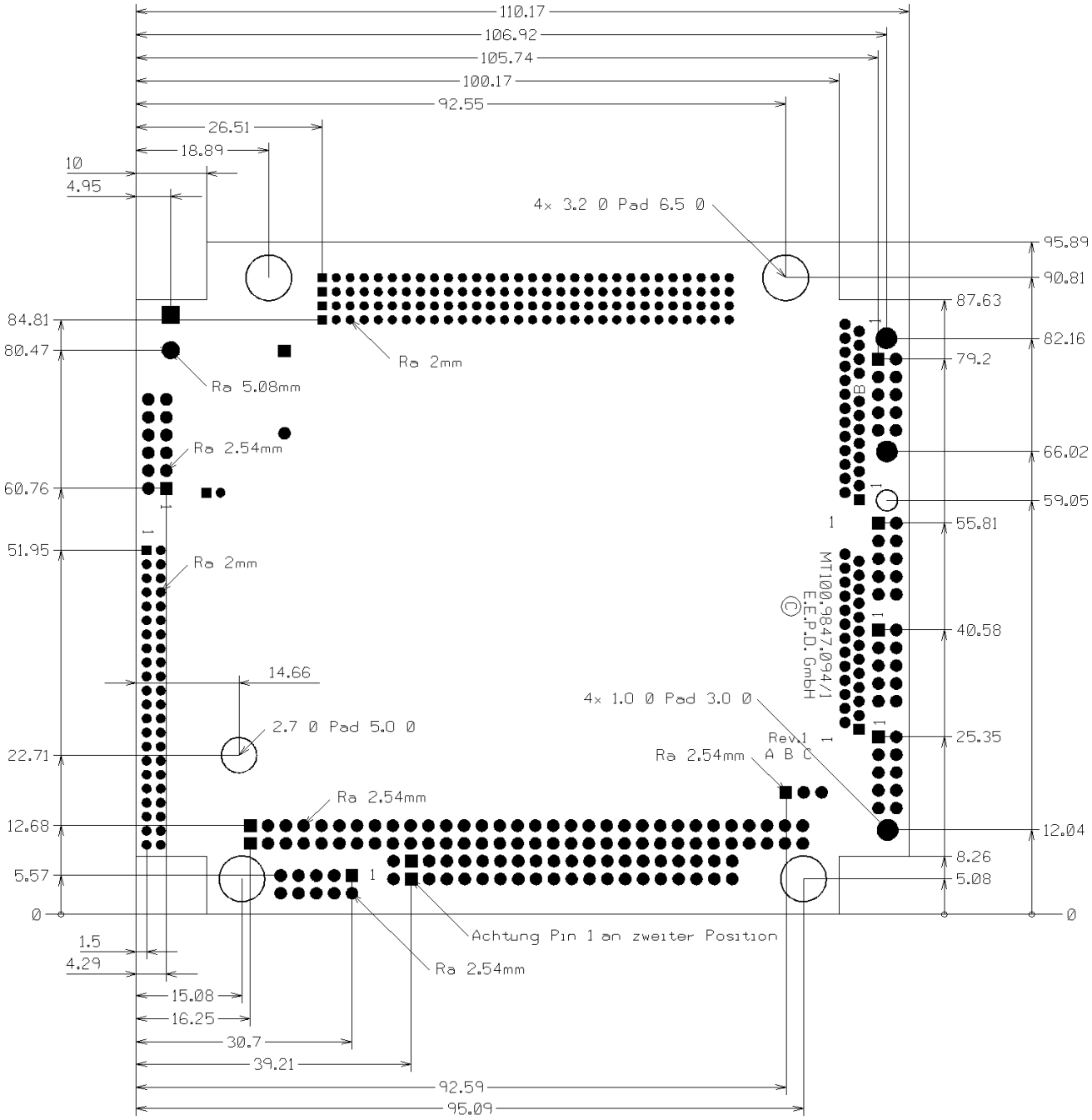
4.2 Dimensions and Connector Location



Dimensions of PROFIVE CPU-T5 (controlling dimension is mm)

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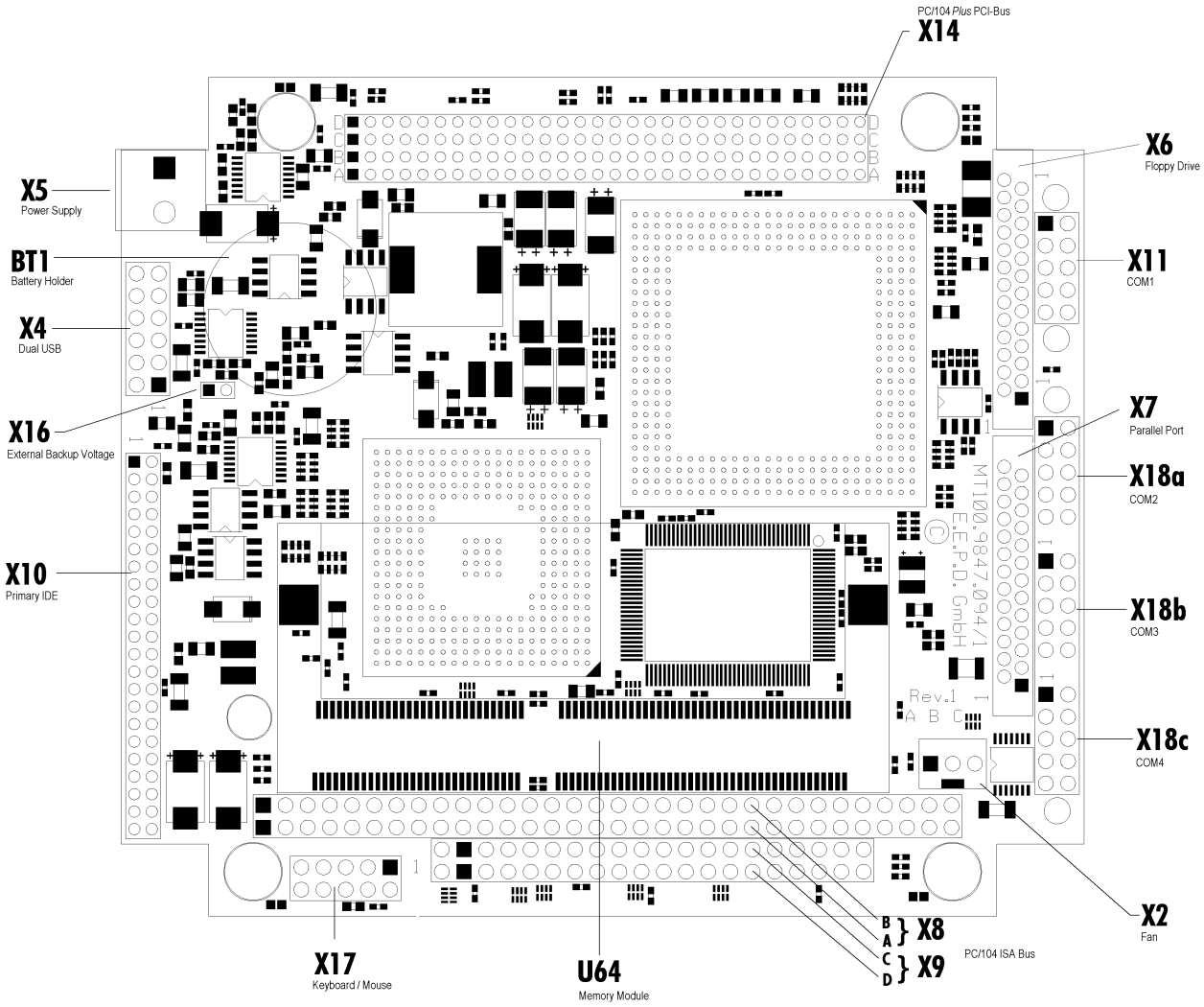

Connector Locations of PROFIVE CPU-T5

4.3 Important Notes

- The signal-high-level voltage on the PC/104 (ISA-Bus) at the CPU-T5 is 3,3V!
- All inputs are 5V tolerant!
- The required minimum signal-high-level voltage according to the IEEE-P996 ISA-bus specification is 2,4V.
- According to this the IEEE-P996 specification is fully met!
- However some ISA-bus-cards are using devices which require a higher signal-voltage than 3,3V as a minimum high-level signal-voltage in order to function properly. These boards are NOT IEEE-P996 compatible and therefore not supported by the CPU-T5.

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- If you experience problems with PC/104 ISA-bus-cards please contact the supplier and/or manufacturer of this card to see if this card is IEEE-P996 compatbile or not.

5 Installation

Before you start
read this chapter completely
make sure that your power supply and all cables meet the requirements of the PROFIVE® CPU-T5 motherboard

SWITCH O F F YOUR POWER SUPPLY!!

5.1 Connecting Power

The board is working with a single +5V power supply. The power supply must meet the following requirements

- Voltage: +5V ± 5% (4,75V...5,25V)
- Current: additionally to the average current consumption the power supply must be capable of current peaks up to 5A
- A peak current of 5A can occur when a system is waked up from a deep power down mode.
- Furthermore the power supply must be able to maintain a stable output within the specified range for load cycling from 50% to 100% within a frequency range from DC to 20MHz.

For pinout of the PC/104 (ISA) or the PC/104-*Plus* (PCI) bus see appendix
Power must be connected separately in order to meet the PC/104-Plus specifications regarding the power consumption of each single board in the stack and the available current through all of the the PC/104 connectors.
We recommend to use a flexible, wire with low impedance and a cross section of at least 1.5 mm^2.

5.2 Inserting Lithium Backup-Battery Coin-Cell

Place the supplied battery (1620) into the battery holder BT1 the plus marking of the battery must be facing up. Alternatively an external lithium battery (3 or 3.6 Volts) can be connected to X16. For description of polarity see appendix.
The coin-cell should last between 3 and 5 Years depending on the actual on-time of the system and the ambient temperature.
A longer on-time will give a longer battery life because there is no current flow out of the battery during power-on.
A higher ambient temperature will give a shorter battery life due to a higher self discharge of the battery when hot.
As replacement use a 1620 coin-cell or any equivalent type.

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5.3 Memory Module Installation

Insert Memory Module into socket U64.
The CPU-T5 motherboard requires DIMM-SO-II compatible memory modules with the following specifications:

- PC-66 compatible
- 3,3 V operating voltage
- DIMM-SO
- 144-pin
- 72mm length
- 25,4mm width
- EDO with 60ns or unbuffered SDRAM with 10ns

5.4 Adding Other PC/104-*Plus* or PC/104 Modules

When adding PC/104-Plus modules to the PROFIVE® CPU-T5 board please note:

- The PROFIVE® CPU-T5 must be at the top of the PC/104-*Plus* bus.
- The first PC/104-*Plus* module below the PROFIVE® CPU-T5 must select 0 or 4 at the rotary switch for the routing of the signals IDSEL, CLK, IRQ, REQ and GNT
- The second PC/104-*Plus* module below the PROFIVE® CPU-T5 must select 1 or 5 at the rotary switch for the routing of the signals IDSEL, CLK, IRQ, REQ and GNT
- The third PC/104-*Plus* module below the PROFIVE® CPU-T5 must select 2 or 6 at the rotary switch for the routing of the signals IDSEL, CLK, IRQ, REQ and GNT
- The fourth PC/104-*Plus* module below the PROFIVE® CPU-T5 must select 3 or 7 at the rotary switch for the routing of the signals IDSEL, CLK, IRQ
- For the fourth module there is no DMA-Bus-Master support available according to the PC/104-*Plus* specification.
- When you have a system with 4 additional PC/104-Plus modules we recommend to use the graphics board as the fourth module because they normally don't use DMA-Bus-Master transfers.
- The PC/104 ISA-Bus can be extended in both directions upward or downward regarding the PROFIVE® CPU-T5 as the middle of the stack.
- The PROFIVE® CPU-T5 supports up to 5 PC/104 ISA-Board in addition to the four PC/104-*Plus* PCI-Boards

When installing PC/104-*Plus* modules for the routing of the signals IDSEL, CLK, IRQ, REQ and GNT must be selected by rotary switch S1. The rotary switch must be adjusted depending on the position of the module within the PC/104-*Plus* stack.
The first module on the stack (the one nearest to the CPU) must select 0 or 4, the second must select 1 or 5 the third must select 2 or 6 and the fourth must select 3 or 7.
For the Ethernet Board selection 3 or 7 is not supported due to the PC/104-Plus specification which states that there is no Bus-Mastering supported for the fourth module.

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6 BIOS Setup Documents

6.1 Introduction To Setup

This manual describes the Award BIOS Setup program. The Setup program lets you modify basic system configuration settings. The settings are stored in a dedicated battery-backed memory, called CMOS RAM, that retains the information when the power is turned off.

The Award BIOS in your computer is a customized version of an industry-standard BIOS for IBM PC AT-compatible personal computers. It supports Intel Pentium and compatible processors. The BIOS provides critical low-level support for the system central processing, memory, and I/O subsystems.

The Award BIOS has been customized by adding important, but non standard, features such as virus and password protection, power management, and detailed fine-tuning of the chipset controlling the system.

The rest of this manual is intended to guide you through the process of configuring your system using Setup.

6.2 Starting Setup

The Award BIOS is immediately activated when you first turn on the computer. The BIOS reads system configuration information in CMOS RAM and begins the process of checking out the system and configuring it through the power-on self test (POST).

When these preliminaries are finished, the BIOS seeks an operating system on one of the data storage devices (hard drive, floppy drive, etc.). The BIOS launches the operating system and hands control of system operations to it.

To start Setup, press the “Del” or “Entf” key some time before or while a message similar to this appears briefly at the bottom of the screen during POST:

TO ENTER SETUP PRESS Del

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If the message disappears before you press “Del” or “Entf” and you still wish to enter Setup, reboot the system.

6.2.1 Setup Keys

These keys help you navigate in Setup:

Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item in the left hand
Right arrow	Move to the item in the right hand
Esc	Main Menu: Quit and not save changes into CMOS RAM. Other pages: Exit current page and return to Main Menu
PgUp	Increase the numeric value or make changes
PgDn	Decrease the numeric value or make changes
+	Increase the numeric value or make changes
-	Decrease the numeric value or make changes
F1	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2	Change color from total 16 colors. F2 to select Shift-F2 color forward, Shift-F2 to select color backward
F3	Calendar, only for Status Page Setup Menu
F4	Reserved
F5	Restore the previous CMOS value from CMOS, only for Option Page Setup Menu

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F6	Load the default CMOS RAM value from BIOS default table, only for Option Page Setup Menu
F7	Load the default
F8	Reserved
F9	Reserved
F10	Save all the CMOS changes, only for Main Menu

6.2.2 Getting Help

Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press Esc or the F1 key again.

6.2.3 In Case of Problems

If, after making and saving system changes with Setup, you discover that your computer no longer is able to boot, the Award BIOS supports an override to the CMOS settings that resets your system to its default configuration.

You can invoke this override by immediately pressing “Ins” or “Einfg” key; when you restart your computer. You can restart by either using the ON/OFF switch, the RESET button or by pressing “Ctrl-Alt-Delete”.

The best advice is to alter only settings that you thoroughly understand.
In particular, do not change settings in the Chipset screen without a good reason. The Chipset defaults have been carefully chosen for the best performance and reliability. Even a seemingly small change to the Chipset setup may causing the system to become unstable.

6.3 Main Setup Menu

When you enter the Award BIOS CMOS Setup Utility, a Main Menu appears on the screen. The Main Menu allows you to select from several Setup functions and two exit choices. Use the arrow keys to select among the items and press Enter to accept and enter the sub-menu.

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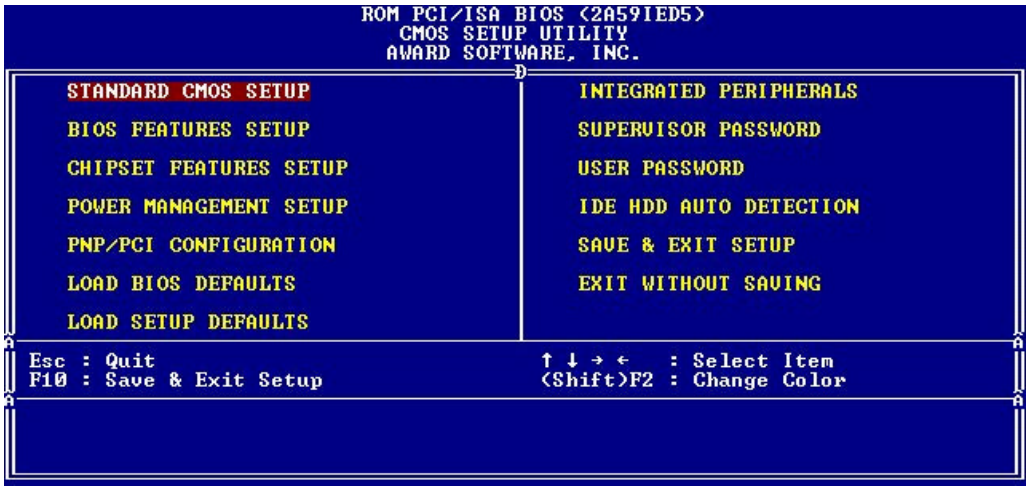
A brief description of each highlighted selection appears at the bottom of the screen.



Main Setup Menu

Following is a brief summary of each Setup category.

Standard CMOS	Options in the original PC AT-compatible BIOS.
BIOS Features	Award enhanced BIOS options.
Chipset Features	Options specific to your system chipset.
Power Management	Advanced Power Management (APM) options.
PnP/PCI Configuration	Plug and Play standard and PCI Local Bus configuration options
Integrated Peripherals	I/O subsystems that depend on the integrated peripherals controller in your system.
Supervisor/User Password Setting	Change, set, or disable a password. In BIOS versions that allow separate user and supervisor passwords, only the supervisor password permits access to Setup. The user password generally allows only power-on access.
IDE HDD Auto Detection	Automatically detect and configure IDE hard disk parameters.
Load BIOS Defaults	BIOS defaults are factory settings for the most stable, minimal-performance system operations.
Load Setup Defaults	Setup defaults are factory settings for optimal-performance system operations.
Save & Exit Setup	Save settings in nonvolatile CMOS RAM and exit Setup.
Exit Without Save	Abandon all changes and exit Setup.

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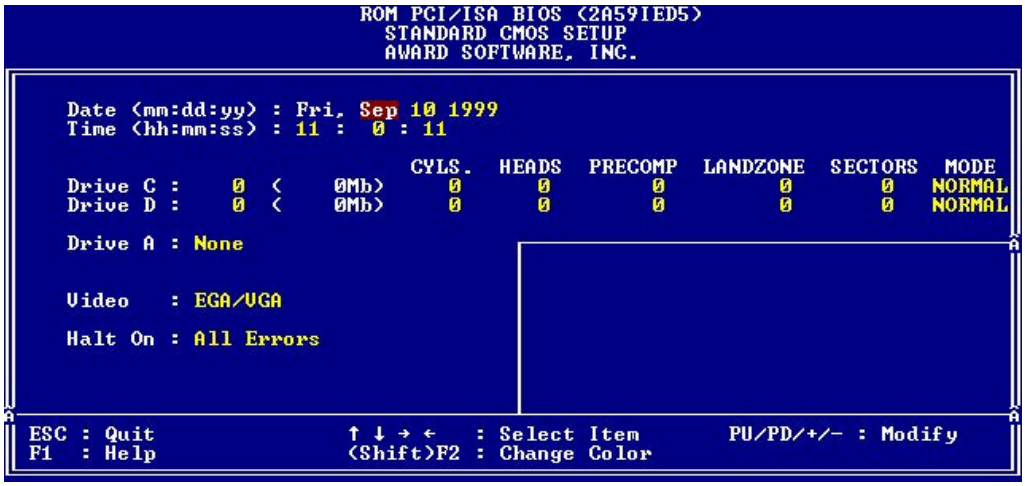
6.4 Standard CMOS Setup



Standard CMOS Setup Menu

In the Standard CMOS menu you can set the system clock and calendar, record disk drive parameters and the video subsystem type, and select the type of errors that stop the BIOS POST.

6.4.1 Date

The BIOS determines the day of the week from the other date information.
This field is for information only.

Press the left or right arrow key to move to the desired field (date, month, year). Press the “PgUp” or “PgDn” key to increment the setting, or type the desired value into the field.

6.4.2 Time

The time format is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Press the left or right arrow key to move to the desired field. Press the “PgUp” or “PgDn” key to increment the setting, or type the desired value into the field.

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6.4.3 HARD DISKS

The BIOS supports up to two IDE drives. This section does not show information about other IDE devices, such as a CD-ROM drive, or about other hard drive types, such as SCSI drives.

NOTE: We recommend that you select type AUTO for all drives.

The BIOS can automatically detect the specifications and optimal operating mode of almost all IDE hard drives. When you select type AUTO for a hard drive, the BIOS detects its specifications during POST, every time the system boots.

If you do not want to select drive type AUTO, other methods of selecting the drive type are available:

1. Match the specifications of your installed IDE hard drive(s) with the preprogrammed values for drive types 1 through 45.
2. Select USER and enter values into each drive parameter field.
3. Use the IDE HDD AUTO DECTECTION function in Setup.

Here is a brief explanation of drive specifications:

* Type: The BIOS contains a table of pre-defined drive types. Each defined drive type has a specified number of cylinders, number of heads, write precompensation factor, landing zone, and number of sectors. Drives whose specifications do not accommodate any pre-defined type are classified as type USER.
* Size: Disk drive capacity (approximate). Note that this size is usually slightly greater than the size of a formatted disk given by a disk-checking program.
* Cyls: Number of cylinders
* Head: Number of heads
* Precomp: Write precompensation cylinder
* Landz: Landing zone
* Sector: Number of sectors
* Mode: Auto, Normal, large, or LBA

    o Auto: The BIOS automatically determines the optimal mode.
    o Normal: Maximum number of cylinders, heads, and sectors supported are 1024, 16, and 63.

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o Large: For drives that do not support LBA and have more than 1024 cylinders.

o LBA (Logical Block Addressing): During drive accesses, the IDE controller transforms the data address described by sector, head, and cylinder number into a physical block address, significantly improving data transfer rates. For drives with greater than 1024 cylinders.

6.4.4 Drive A / Drive B

Select the correct specifications for the diskette drive(s) installed in the computer.

None	No diskette drive installed
360K	5.25 in 5-1/4 inch PC-type standard drive; 360 kilobyte capacity
1.2M	5.25 in 5-1/4 inch AT-type high-density drive; 1.2 megabyte capacity
720K	3.5 in 3-1/2 inch double-sided drive; 720 kilobyte capacity
1.44M	3.5 in 3-1/2 inch double-sided drive; 1.44 megabyte capacity
2.88M	3.5 in 3-1/2 inch double-sided drive; 2.88 megabyte capacity

6.4.5 Video

Select the type of primary video subsystem in your computer. The BIOS usually detects the correct video type automatically.

EGA/VGA	Enhanced Graphics Adapter/Video Graphics Array. For EGA, VGA, SEGA, SVGA or PGA monitor adapters.
CGA 40	Color Graphics Adapter, power up in 40 column mode.
CGA 80	Color Graphics Adapter, power up in 80 column mode.
MONO	Monochrome adapter, includes high resolution monochrome adapters.

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6.4.6 Halt On

During the power-on self-test (POST), the computer stops if the BIOS detects a hardware error. You can tell the BIOS to ignore certain errors during POST and continue the boot-up process. These are the selections:

No errors	POST does not stop for any errors.
All errors	If the BIOS detects any non-fatal error, POST stops and prompts you to take corrective action.
All, But Keyboard	POST does not stop for a keyboard error, but stops for all other errors.
All, But Diskette	POST does not stop for diskette drive errors, but stops for all other errors.
All, But Disk/Key	POST does not stop for a keyboard or disk error, but stops for all other errors.

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6.4.7 Memory

You cannot change any values in the Memory fields; they are only for your information. The fields show the total installed random access memory (RAM) and amounts allocated to base memory, extended memory, and other (high) memory. RAM is counted in kilobytes (KB: approximately one thousand bytes) and megabytes (MB: approximately one million bytes).

RAM is the computer's working memory, where the computer stores programs and data currently being used, so they are accessible to the CPU.

* Base Memory

  Typically 640 KB. Also called conventional memory. The DOS operating system and conventional applications use this area.

* Extended Memory

  Above the 1-MB boundary. Early IBM personal computers could not use memory above 1 MB, but current PCs and their software can use extended memory.

* Other Memory

  Between 640 KB and 1 MB; often called High memory. DOS may load terminate-and-stay-resident (TSR) programs, such as device drivers, in this area, to free as much conventional memory as possible for applications. Lines in your CONFIG.SYS file that start with LOADHIGH load programs into high memory.

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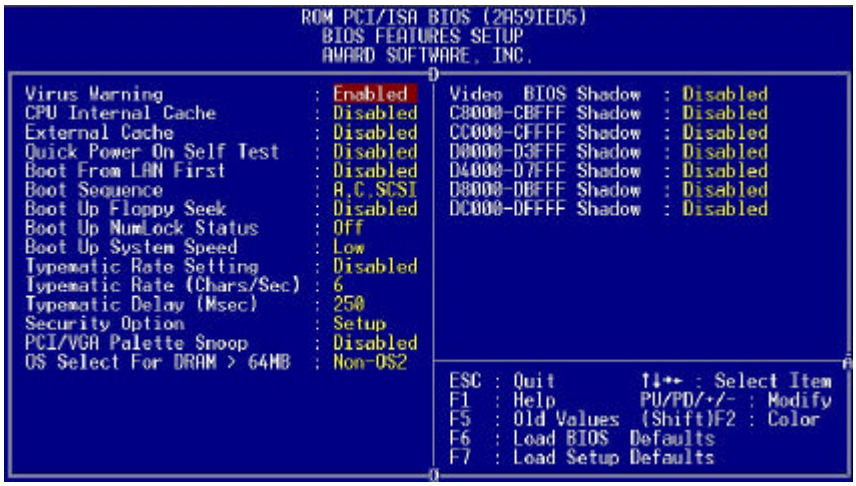
6.5 BIOS Features Setup



BIOS Features Setup

This screen contains industry-standard options additional to the core PC AT BIOS. This section describes all fields offered by Award Software in this screen. Some fields may vary from those in your Setup program or may have been removed.

6.5.1 Virus Warning

When enabled, you receive a warning message if a program (specifically, a virus) attempts to write to the boot sector or the partition table of the hard disk drive. You should then run an anti-virus program. Keep in mind that this feature protects only the boot sector, not the entire hard drive.

NOTE: Many disk diagnostic programs that access the boot sector table can trigger the virus warning message. If you plan to run such a program, we recommend that you first disable the virus warning.

6.5.2 CPU Internal Cache / External Cache

Cache memory is additional memory that is much faster than conventional DRAM (system memory). The Pentium CPUs contain internal cache memory, and the CPU-T5 has additional 512KB (external) cache memory. When the CPU requests data, the system

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transfers the requested data from the main DRAM into cache memory, for even faster access by the CPU.

The External Cache field may not appear if your system does not have external cache memory.

6.5.3 Quick Power On Self Test

Select Enabled to reduce the amount of time required to run the power-on self-test (POST). A quick POST skips certain steps. We recommend that you normally disable quick POST. Better to find a problem during POST than lose data during your work.

6.5.4 Boot from LAN first

If DISABLED, CPU-T5 will boot as designated in BOOT SEQUENCE. If ENABLED CPU-T5 tries to boot from a network via network adapter with BootPROM.

6.5.5 Boot Sequence

The original IBM PCs loaded the DOS operating system from drive A (floppy disk), so IBM PC-compatible systems are designed to search for an operating system first on drive A, and then on drive C (hard disk). However, the BIOS now offers many different boot sequence options of three drives each. In addition to the traditional drives A and C, options include IDE hard drives D, E, and F; plus a SCSI hard drive and a CD-ROM drive.

6.5.6 Boot Up Floppy Seek

When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360-KB floppy drives have 40 tracks; drives with 720 KB, 1.2 MB, and 1.44 MB capacity all have 80 tracks. Because very few modern PCs have 40-track floppy drives, we recommend that you set this field to Disabled to save time.

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6.5.7 Boot Up NumLock Status

Toggle between On or Off to control the state of the NumLock key when the system boots. When toggled On, the numeric keypad generates numbers instead of controlling cursor operations.

6.5.8 Boot Up System Speed

Select High to boot at the default CPU speed; select Low to boot at the speed of the AT bus. Some add-in peripherals or old software (such as old games) may require a slow CPU speed. The default setting is High.

6.5.9 Typematic Rate Setting

When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system.

When Enabled, you can select a typematic rate and typematic delay.

6.5.10 Typematic Rate (Chars/Sec)

When the typematic rate setting is enabled, you can select a typematic rate (the rate at which character repeats when you hold down a key) of 6, 8, 10,12, 15, 20, 24 or 30 characters per second.

6.5.11 Typematic Delay (Msec)

When the typematic rate setting is enabled, you can select a typematic delay (the delay before key strokes begin to repeat) of 250, 500, 750 or 1000 milliseconds.

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6.5.12 Security Option

If you have set a password, select whether the password is required every time the System boots, or only when you enter Setup.

6.5.13 PCI/VGA Palette Snoop

Your BIOS Setup many not contain this field. If the field is present, leave at Disabled.

6.5.14 OS Select for DRAM > 64MB

Select OS2 only if you are running OS/2 operating system with greater than 64 MB of RAM on your system.

6.5.15 Shadow

Software that resides in a read-only memory (ROM) chip on a device is called firmware. The Award BIOS permits shadowing of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals, such as, for example, a SCSI adaptor.

Shadowing copies firmware from ROM into system RAM, where the CPU can read it through the 16-bit or 32-bit DRAM bus. Firmware not shadowed must be read by the system through the 8-bit X-bus. Shadowing improves the performance of the system BIOS and similar ROM firmware for expansion peripherals, but it also reduces the amount of high memory (640 KB to 1 MB) available for loading device drivers, etc.

Enable shadowing into each section of memory separately. The System BIOS System is always shadowed.

Video BIOS shadows into memory area C0000-C7FFF. The remaining areas shown on the BIOS Features Setup screen may be occupied by other expansion card firmware. If an

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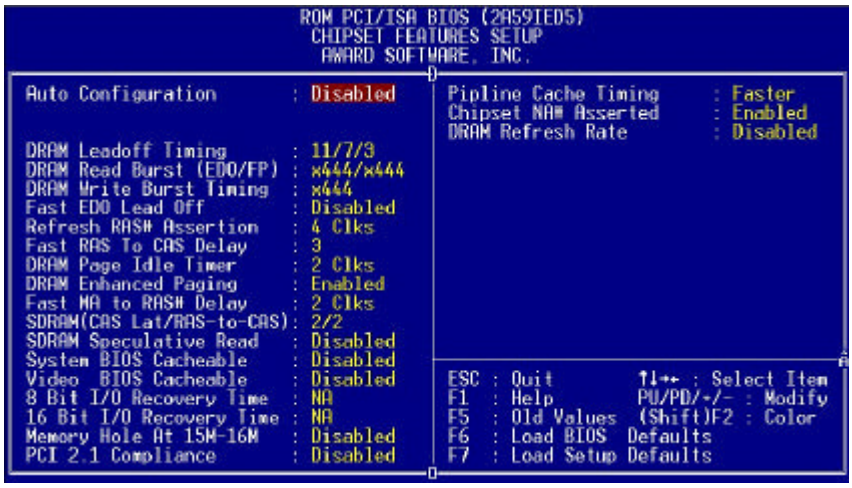
expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM.



6.6 Chipset Features Setup

Chipset Features Setup

This section describes features of the Intel 82430TX PCIset.

ADVANCED OPTIONS

The parameters in this screen are for system designers, service personnel, and technically competent users only. Do not reset these values unless you understand the consequences of your changes.

NOTE: This chapter describes all fields offered by Award Software in this screen. On your CPU-T5 some options may have been omitted or modified.

6.6.1 Auto Configuration

Auto Configuration selects predetermined optimal values of chipset parameters. When Disabled, chipset parameters revert to setup information stored in CMOS. Many fields in this screen are not available when Auto Configuration is Enabled.

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6.6.2 DRAM Timing

The value in this field depends on performance parameters of the installed memory chips (DRAM). Do not change the value from the factory setting unless you install new memory that has a different performance rating than the original DRAMs.

6.6.3 DRAM Leadoff Timing

Select the combination of CPU clocks the DRAM on your board requires before each read from or write to the memory. Changing the value from the setting determined by the board designer for the installed DRAM may cause memory errors.

6.6.4 DRAM Read Burst (EDO)

Sets the timing for reads from EDO (Extended Data Output) memory. The lower the timing numbers, the faster the system addresses memory. Selecting timing numbers lower than the installed DRAM is able to support can result in memory errors.

6.6.5 DRAM Write Burst Timing

Sets the timing for writes to memory. The lower the timing numbers, the faster the system addresses memory. Selecting timing numbers lower than the installed DRAM is able to support can result in memory errors.

6.6.6 Fast EDO Lead Off

Select Enabled only for EDO DRAMs in either a synchronous cache or a cacheless system. It causes a 1-HCLK pull-in for all read leadoff latencies for EDO DRAMs (i.e., page hits, page misses, and row misses). FPM DRAMs are not supported with the CPU-T5.

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6.6.7 Refresh RAS# Assertion

Select the number of clock ticks RAS# is asserted for refresh cycles.

6.6.8 Fast RAS# to CAS# Delay

When DRAM is refreshed, both rows and columns are addressed separately.
This field lets you insert a timing delay between the CAS and RAS strobe signals, used when DRAM is written to, read from, or refreshed. Disabled gives faster performance; Enabled give more stable performance.

6.6.9 DRAM Page Idle Timer

Select the amount of time in HCLKs that the DRAM controller waits to close a DRAM page after the CPU becomes idle.

6.6.10 DRAM Enhanced Paging

When Enabled, the chipset keeps the page open until a page/row miss. When Disabled, the chipset uses additional information to keep the DRAM page open when the host may be "right back."

6.6.11 Fast MA to RAS# Delay CLK

The values in this field are set by the system board designer, depending on the DRAM installed. Do not change the values in this field unless you change specifications of the installed DRAM or the installed CPU.

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6.6.12 SDRAM (CAS Lat/RAS-to-CAS)

You can select a combination of CAS latency and RAS-to-CAS delay in HCLKs of 2/2 or 3/3. The system board designer should set the values in this field, depending on the DRAM installed. Do not change the values in this field unless you change specifications of the installed DRAM or the installed CPU.

6.6.13 SDRAM Speculative Read

The chipset can "speculate" on a DRAM read address, thus reducing read latencies. The CPU issues a read request containing the data memory address. The DRAM controller receives the request. When this field is Enabled, the controller issues the read command slightly before it has finished decoding the data address.

6.6.14 System BIOS Cacheable

Selecting Enabled allows caching of the system BIOS ROM at F0000h-FFFFFh, resulting in better system performance. However, if any program writes to this memory area, a system error may result.

6.6.15 Video BIOS Cacheable

Selecting Enabled allows caching of the video BIOS ROM at C0000h to C7FFFh, resulting in better video performance. However, if any program writes to this memory area, a system error may result.

6.6.16 8/16 Bit I/O Recovery Time

The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is so much faster than the ISA bus.

These two fields let you add recovery time (in bus clock cycles) for 16-bit and 8-bit I/O.

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6.6.17 Memory Hole at 15M-16M

You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.

6.6.18 PCI 2.1 Compliance

PCI 2.1 Compliance can be enabled or disabled.

6.6.19 Pipeline Cache Timing

Select Faster if your system contains one bank of pipelined burst SRAM. Select Fastest if your system contains two banks of pipelined burst SRAM.

6.6.20 Chipset NA# Asserted

When Disabled, NA# assertion is dependent on the cache type and size. When Enabled, the NA# pin never asserted. Selecting Enabled permits pipelining, in which the chipset signals the CPU for a new memory address before all data transfers for the current cycle are complete, resulting in faster performance.

6.6.21 DRAM Refresh Rate

Select the period required to refresh the DRAMs, according to DRAM specifications.

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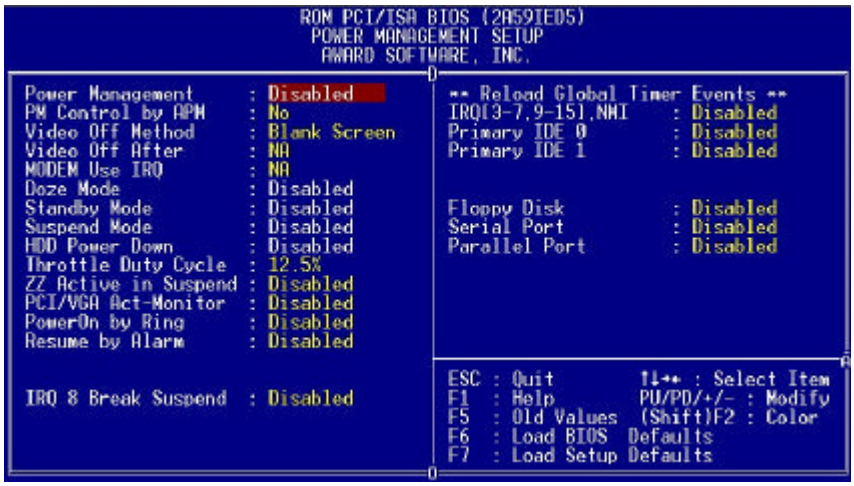
6.7 Power Management



Power Management

NOTE: This chapter describes all fields offered by Award Software in this screen. Your system board designer may omit or modify some fields.

6.7.1 Power Management

This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. See the section PM Timers for a brief description of each mode.

This table describes each power management mode:

*Max Saving	Maximum power savings. Only Available for SL CPUs. Inactivity period is 1 minute in each mode.
*User Define	Set each mode individually. Select time-out periods in the PM Timers section, following.
*Min Saving	Minimum power savings. Inactivity period is 1 hour in each mode (except the hard drive).

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6.7.2 PM Control by APM

If Advanced Power Management (APM) is installed on your system, selecting Yes gives better power savings.

6.7.3 Video Off Method

Determines the manner in which the monitor is blanked.

V/H SYNC+Blank	System turns off vertical and horizontal synchronization ports and writes blanks to the video buffer.
DPMS Support	Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values.
Blank Screen	System only writes blanks to the video buffer.

6.7.4 Video Off After

As the system moves from lesser to greater power-saving modes, select the mode in which you want the monitor to blank.

6.7.5 MODEM uses IRQ

When not NA, displayed IRQ brings CPU to normal operation.

6.7.6 Doze Mode

After the selected period of system inactivity (1 minute to 1 hour), the CPU clock runs at slower speed while all other devices still operate at full speed.

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6.7.7 Standby Mode

After the selected period of system inactivity (1 minute to 1 hour), the fixed disk drive and the video shut off while all other devices still operate at full speed.

6.7.8 Suspend Mode

After the selected period of system inactivity (1 minute to 1 hour), all devices except the CPU shut off.

6.7.9 HDD Power Down

After the selected period of drive inactivity (1 minute to 15 minutes), the hard disk drive powers down while all other devices remain active.

6.7.10 Throttle Duty Cycle

When the system enters Doze mode, the CPU clock runs only part of the time.
You may select the percent of time that the clock runs.

6.7.11 PCI/VGA Active Monitor

When Enabled, any video activity restarts the global timer for Standby mode.

6.7.12 Power on by Ring

When Enabled, the CPU resumes to normal operation by detecting 'Ring Indication'.

6.7.13 Resume by Alarm

When Enabled, the CPU resumes to normal operation by detecting an alarm.

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6.7.14 IRQ8 Clock Event

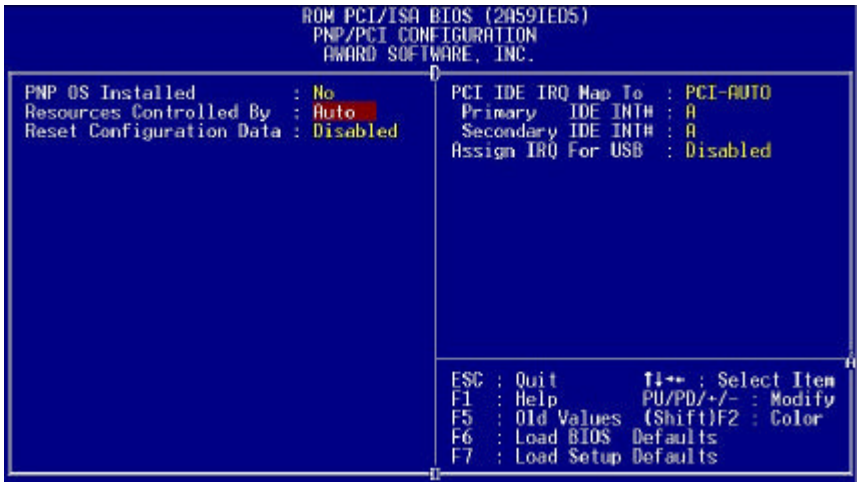
You can turn On or Off monitoring of IRQ8 (the Real Time Clock) so it does not awaken the system from Suspend mode.

6.7.15 Reload Global Timer Events

When Enabled, an event occurring on each device listed below restarts the global time for Standby mode.

IRQ3 -7, 9-15, NMI	Enabled
Primary IDE 0	Disabled
Primary IDE 1	Disabled
Secondary IDE 0	Disabled
Secondary IDE 1	Disabled
Floppy Disk	Disabled
Serial Port	Enabled
Parallel Port	Disabled

6.8 PnP/PCI Configuration



PnP/PCI Configuration

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NOTE: This chapter describes all fields offered by Award Software in this screen. Your system board designer may omit or modify some fields.

6.8.1 PNP OS Installed

Select Yes if the system operating environment is Plug-and-Play aware (e.g., Windows 95 / Windows 98).

6.8.2 Resources Controlled By

The Award Plug and Play BIOS can automatically configure all the boot and Plug and Play-compatible devices. If you select Auto, all the interrupt request (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them.

6.8.3 Reset Configuration Data

Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

6.8.4 IRQ n Assigned to

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt:

Legacy ISA Devices compliant with the original PC AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).

PCI/ISA PnP Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

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6.8.5 DMA n Assigned to

When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the interrupt:

Legacy ISA Devices compliant with the original PC AT bus specification, requiring a specific DMA channel.

PCI/ISA PnP Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

6.8.6 PCI IDE IRQ Map to

This field lets you select PCI IDE IRQ mapping or PC AT (ISA) interrupts. If your system does not have one or two PCI IDE connectors on the system board, select values according to the type of IDE interface(s) installed in your system (PCI or ISA). Standard ISA interrupts for IDE channels are IRQ14 for primary and IRQ15 for secondary.

6.8.7 Primary/Secondary IDE INT#

Each PCI peripheral connection is capable of activating up to four interrupts: INT# A, INT# B, INT# C and INT# D. By default, a PCI connection is assigned INT# A. Assigning INT# B has no meaning unless the peripheral device requires two interrupt services rather than just one. Because the PCI IDE interface in the chipset has two channels, it requires two interrupt services. The primary and secondary IDE INT# fields default to values appropriate for two PCI IDE channels, with the primary PCI IDE channel having a lower interrupt than the secondary.

6.8.8 Assign IRQ For USB

IRQ can be assigned for USB Port in PIIX4.

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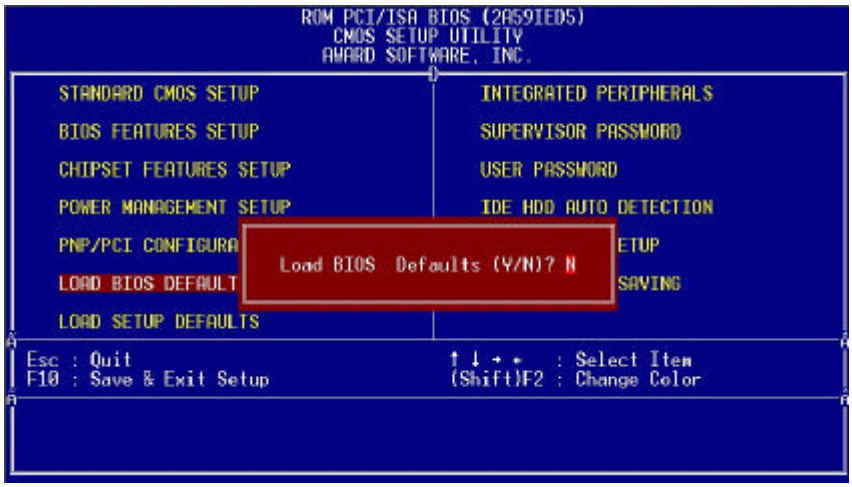
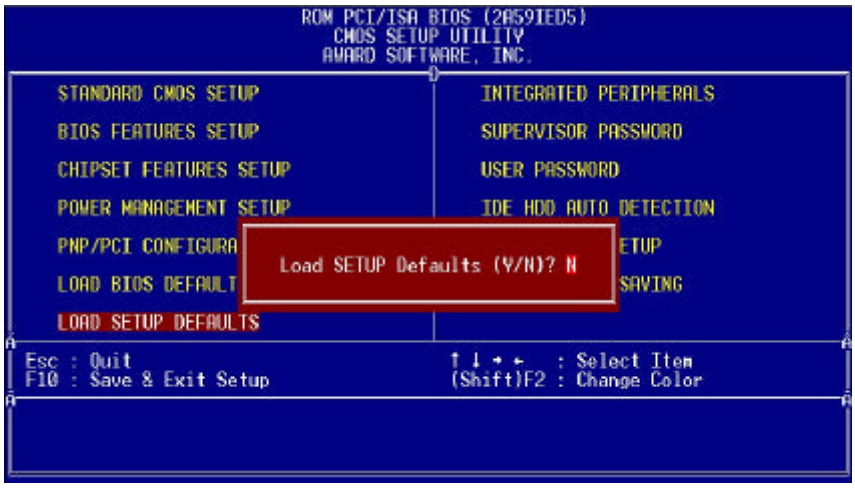
6.9 Load BIOS Defaults



Note: In case of misprogramming the settings, this defaults will bring all settings to their origin values. Harddisks and Floppydrives will be deleted!

6.10 Load Setup Defaults



Note: In case of misprogramming the settings or changing backup battery, this defaults will bring all settings to their origin values. Floppydrive will be set to 1.44MB/3.5“ , HD will be set to Autodetect.

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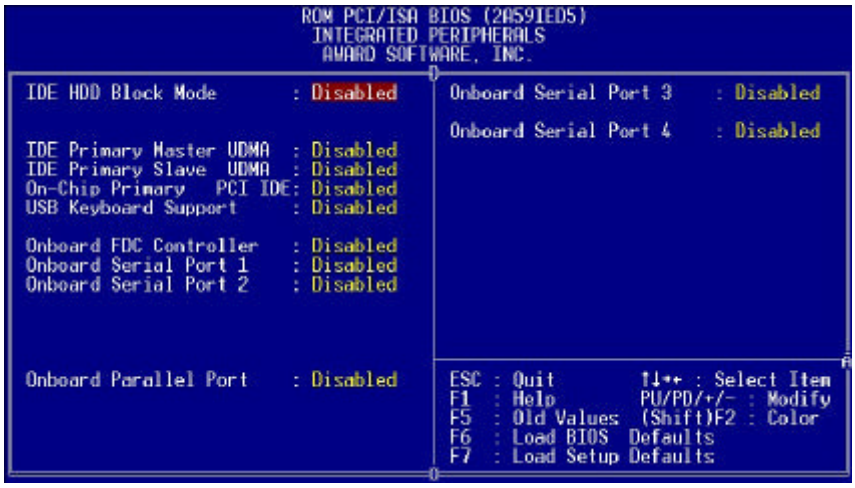
6.11 Integrated Peripherals

NOTE: This chapter describes all fields offered by Award Software in this screen. On your CPU-T5 some fields may have been omitted or modified.



Integrated Peripherals

6.11.1 IDE HDD Block Mode

Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.

6.11.2 IDE Primary Master/Slave PIO

The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device.

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6.11.3 IDE Primary Master/Slave UDMA

Ustra DMA/33 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support Ultra DMA/33, select Auto to enable BIOS support.

6.11.4 On-Chip Primary PCI IDE

The integrated peripheral controller contains an IDE interface with support for two IDE channels. Select Enabled to activate each channel separately.

6.11.5 USB Keyboard Support

Select Enabled if your system contains a Universal Serial Bus (USB) controller and you have a USB keyboard.

6.11.6 Onboard FDC Controller

Select Enabled if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install an add-in FDC or the system has no floppy drive, select Disabled in this field.

6.11.7 Onboard Serial Port 1/ Onboard Serial Port 2

Serial Ports can be configured as COM1.. COM4, Auto or Disabled.
Possible settings are: Auto, Disabled, 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4 and 2E8/IRQ3.

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6.11.8 Onboard UART 2 Mode

The second serial port offers these InfraRed interface modes:

*HPSIR	IrDA-compliant serial infrared port
*ASK-IR	Amplitude shift keyed infrared port
*IrDA 1.0	IrDA serial infrared port 1.0
*IrDA 1.1	IrDA serial infrared port 1.1

6.11.9 IR Duplex Mode

Select the value required by the IR device connected to the IR port.
Full-duplex mode permits simultaneous two-direction transmission.
Half-duplex mode permits transmission in one direction only at a time.
If no infrared port is present in the system, select Disabled.

6.11.10 TxD, Rxd Active

Consult your IR peripheral documentation to select the correct setting of the TxD and RxD signals.

6.11.11 IRRX mode Select

Select the value required by the IR device connected to the IR port.
Consult your IR peripheral documentation to select the correct setting of the IRRX signals.
Can be changed between IRMODE or IRRX3-mode.

6.11.12 Onboard Parallel Port

Select a logical LPT port name and matching address for the physical parallel (printer) port.

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6.11.13 Parallel Port Mode

Select an operating mode for the onboard parallel (printer) port. Select Normal unless your hardware and software require one of the other modes offered in this field.

6.11.14 ECP Mode Use DMA

Select a DMA channel for the port.

6.11.15 Onboard Serial Port 3/ Onboard Serial Port 4

Serial Ports can be configured to Portaddress: 0x3F8, 0x2F8, 0x3E8, 0x2E8, 0x130h, 0x1E0h or Disabled.
Possible IRQ settings are: IRQ3, IRQ4, IRQ5, IRQ10 and IRQ11.

6.12 Supervisor & User Password Setting

When you select this function, a message appears at the center of the screen:

ENTER PASSWORD:

Type the password, up to eight characters, and press Enter. Typing a password clears any previously entered password from CMOS memory.

Now the message changes:

CONFIRM PASSWORD:

Again, type the password and press Enter.

To abort the process at any time, press Esc.

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In the Security Option item in the BIOS Features Setup screen, select System or Setup:

*System Enter a password each time the system boots and when ever you enter Setup.

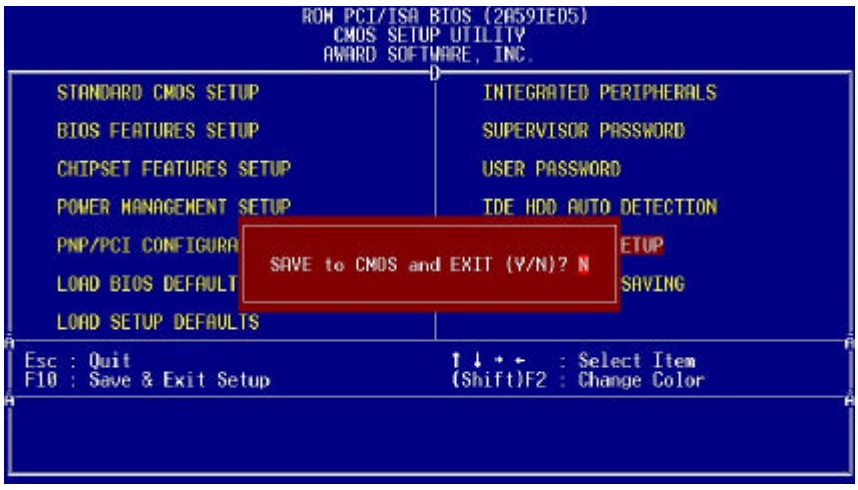
*Setup Enter a password when ever you enter Setup.

NOTE: To clear the password, simply press Enter when asked to enter a password. Then the password function is disabled.

6.13 IDE HDD AUTO DETECTION

Select IDE HDD AUTO DETECTION to check your HDD parameters.
Normally this is not necessary. If there is a malfunction on your HDD, auto detection should be done.

6.14 Save to CMOS and Exit



If you have done all changing, select „Save to CMOS and Exit“ and press the ‚Y‘ key to confirm on US-style keyboards and ‚Z‘ key on German-style keyboards.

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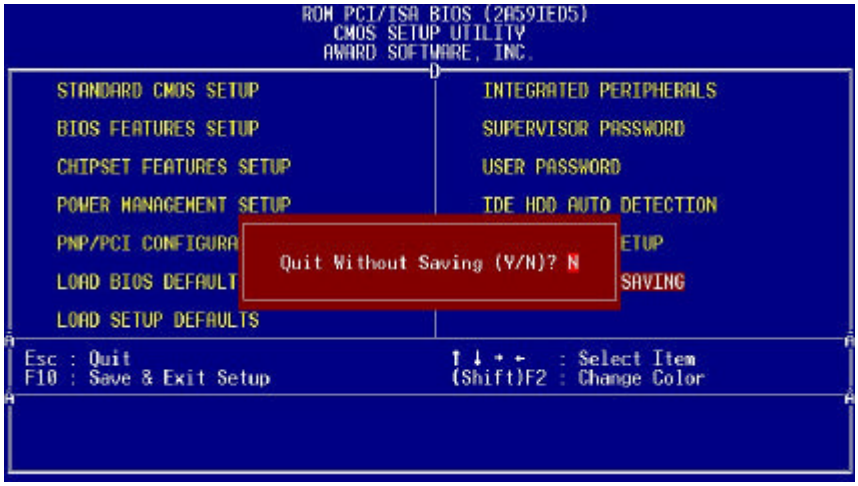
6.15 Quit Without Saving



If you are not sure, everything has been changed the right way, select „Quit Without Saving“ and confirm with the ‚Y‘ key on US-style keyboards and ‚Z‘ on German-style keyboards.

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7 Utility Software

Utility programs for PROFIVE CPU-T5:

Program	Description
CONF_P5.EXE	Program to configure the microcontroller of PROFIVE CPU-T5. With this program you have the ability to **read** or to **modify** this configuration.
WDT_DEMO.EXE	Demo software which shows how to handle the external software watchdog timer and the external hardware watchdog timer.
CONF_ROM.EXE	EEPROM configuration of PROFIVE CPU-T5. With this program you have the ability to load a binary file (size: 256 byte) into the EEPROM of the PROFIVE CPU-T5. The EEPROM is neccessary for configuration of the microcontroller.

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7.1 CONF_P5.EXE

The CONF_P5.EXE is the program to configure the microcontroller of the PROFIVE CPU-T5. You have the ability to read this configuration only or to modify single values of the configuration.

First copy the CONF_P5.EXE file to your hard disk.
After you have installed the EXE-file you can execute the program to configure the microcontroller.

Syntax:

CONF_P5 [Option]

Option:

/? Information
Displays a short information on the screen

If you type CONF_P5 /? you will get the following short information on the screen:

```
-------------------------------------------------------------
Microcontroller Configuration of PROFIVE CPU-Series
Microcontroller Program Version xx
Program CONF_P5, Version x.x

PC/104-Plus PROFIVE CPU-Series Card by E.E.P.D. GmbH, Germany

Copyright (C) 1998 - 2000 by E.E.P.D. GmbH.
All rights reserved.
-------------------------------------------------------------
Address:

E.E.P.D. Electronic Equipment Produktion & Distribution GmbH
Gewerbering 3
D-85258 Weichs, Germany
Tel.: ++49-8136-9328-0
Fax.: ++49-8136-6910
Internet: http://www.eepd.com
-------------------------------------------------------------
```


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If you type CONF_P5 without an option the program is executed. Then you will get the following message in DOS:

```
Find PCI-Device...passed
Find Base-Address...passed
Configure SMBus...done

Set parameter of PROFIVE CPU-Series

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```

CPUVCORE min: x.xx V	CPUVCORE: x.xx V	CPUVCORE max: x.xx V
CPUVIO min: x.xx V	CPUVIO: x.xx V	CPUVIO max: x.xx V
P3V3 min: x.xx V	P3V3: x.xx V	P3V3 max: x.xx V
VCC_MESS min: x.xx V	VCC_MESS: x.xx V	VCC_MESS max: x.xx V

Fan_speed min: x U/min	Temp. act: x C
Fan_speed act: x U/min	Temp. max: x C
Fan_speed max: x U/min	Temp. hys: x C

Pulse per rotation of fan:.....	x
Fan loop:.....	x ms
IRQ on(1)/off(0):.....	x
Using IRQ5(1)/IRQ10(2)/IRQ15(3):.....	x
IRQ low(0)/high(1) active:.....	x
Delay before PWRGD:.....	x ms
Delay before PWRGD at start:.....	x ms
Manual reset delay:.....	x ms
Time to ext. SOFTWARE watchdog timer (WDT) reset.....	x ms
Delay before PWRGD after ext. SOFTWARE WDT reset.....	x ms
Time to ext. HARDWARE watchdog timer (WDT) reset.....	x ms
Delay before PWRGD after ext. HARDWARE WDT reset.....	x ms
Status:.....	x

```
Would you like to change a parameter (p), refresh results (r),
store results in binary file (s) or quit (q):
```

If you type <q> you will quit the program.
If you type <r> the results are refreshed.
If you type <s> the results are stored in a binary file of your choice.
If you type <p> the following message appears:

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```
CPUVCORE min:...x.xx V....1              CPUVCORE max:...x.xx V.....2
CPUVIO   min:...x.xx V....3              CPUVIO   max:...x.xx V.....4
P3V3     min:...x.xx V....5              P3V3     max:...x.xx V.....6
VCC_MESS min:...x.xx V....7              VCC_MESS max:...x.xx V.....8

TEMPERATURE:                             maximal:.........x C.....10
in °C(0) or °F(1):........9              hysterese:........x C.....11

FAN:                                     Fan speed min:....x RPM...13
PPR of fan:.............12              Fan speed max:....x RPM...14

INTERRUPTS:                      High active:..15    Low active:.16
                                 IRQ on:.......17    IRQ off:....18
                   IRQ5:..19     IRQ10:........20    IRQ15:......21

Delay before PWRGD:.................................x * 100 ms..22
Delay before PWRGD at start:........................x * 100 ms..23
Manual reset delay:.................................x * 100 ms..24
Time to ext. SOFTWARE watchdog timer (WDT) reset:.....x * 100 ms..25
Delay before PWRGD after ext. SOFTWARE WDT reset:.....x * 100 ms..26
Time to ext. HARDWARE watchdog timer (WDT) reset:.....x * 100 ms..27
Delay before PWRGD after ext. HARDWARE WDT reset:.....x * 100 ms..28
Clear status byte:..................................................29
Write to EEPROM:....................................................30
Read from EEPROM:...................................................31
NOTHING:...........................................................0

                                                    Your choice:
```

Now you can select the number of the parameter you want to modify. Then you have to enter the new value of the choosen parameter if it is neccessary.

When you have modified all parameter you wanted to change you have to quit the program and to restart your computer for the changes to take effect.

7.1.1 Description of the Parameters

VOLTAGES

1 CPUVCORE min

Minimal value of the voltage CPUVCORE. The microcontroller resets the PROFIVE CPU if CPUVCORE drops below this value. The PROFIVE CPU will not reboot until CPUVCORE exceeds the value of CPUVCORE min.

Microcontroller default value is 0.00 V.
Factory default value is 1.50 V.
Recommended value for Intel Pentium MMX 166 MHz is 1.50 V.
Recommended value for Intel Pentium MMX 266 MHz is 1.70 V.

2 CPUVCORE max

Maximal value of the voltage CPUVCORE. The microcontroller resets the PROFIVE CPU if CPUVCORE exceeds this value. The PROFIVE CPU will not reboot until CPUVCORE drops below the value of CPUVCORE max.

Microcontroller default value is 4.55 V.
Factory default value is 2.28 V.
Recommended value for Intel Pentium MMX 166 MHz is 2.10 V.
Recommended value for Intel Pentium MMX 266 MHz is 2.28 V.

3 CPUVIO min

Minimal value of the voltage CPUVIO. The microcontroller resets the PROFIVE CPU if CPUVIO drops below this value. The PROFIVE CPU will not reboot until CPUVIO exceeds the value of CPUVIO min.

Microcontroller default value is 0.00 V.
Factory default value is 2.09 V.

4 CPUVIO max

Maximal value of the voltage CPUVIO. The microcontroller resets the PROFIVE CPU if CPUVIO exceeds this value. The PROFIVE CPU will not reboot until CPUVIO drops below the value of CPUVIO max.

Microcontroller default value is 4.55 V.
Factory default value is 2.89 V.

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5 P3V3 min

Minimal value of the voltage 3.3 V. The microcontroller resets the PROFIVE CPU if the voltage 3.3 V drops below this value. The PROFIVE CPU will not reboot until this voltage exceeds the value of P3V3 min.

Microcontroller default value is 0.00 V.
Factory default value is 3.00 V.

6 P3V3 max

Maximal value of the voltage 3.3 V. The microcontroller resets the PROFIVE CPU if the voltage 3.3 V exceeds this value. The PROFIVE CPU will not reboot until this voltage fall drops below the value of P3V3 max.

Microcontroller default value is 4.55 V.
Factory default value is 3.78 V.

7 VCC_MESS min

Minimal value of the voltage VCC (5 V). The microcontroller resets the PROFIVE CPU if the voltage VCC (5 V) drops below this value. The PROFIVE CPU will not reboot until this voltage exceeds the value of VCC_MESS min.

Microcontroller default value is 0.00 V.
Factory default value is 4.50 V.

8 VCC_MESS max

Maximal value of the voltage VCC (5 V). The microcontroller resets the PROFIVE CPU if the voltage VCC (5 V) exceeds this value. The PROFIVE CPU will not reboot until this voltage drops below the value of VCC_MESS max.

Microcontroller default value is 5.82 V.
Factory default value is 5.50 V.

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TEMPERATURE

9 in °C (0) or °F (1)

Choice of unit of the temperature. Type „0“ for degrees in celcius or „1“ for degrees in fahrenheit. The default value is 0 for degrees in celcius.

10 maximal

Maximal value of the temperature. The microcontroller sends out an interrupt request (if enabled) if the actual temperature of the CPU exceeds this value. The default value is 120 °C.

Further on the digital temperature sensor asserts the THRM-signal at the PIIX4 of the PROFIVE CPU when the actual temperature exceeds the value of the maximal temperature.

11 hysterese

Hysterese temperature of digital temperature sensor. Default value is 110 °C.

The THRM-signal at the PIIX4 of the PROFIVE CPU is deactivated by the digital temperature sensor when the actual temperature drops below the hysterese temperature.

FAN

12 PPR of fan

Pulse per rotation of the fan. Specifies the number of pulses per rotation the used fan sends out.

Microcontroller default value is 1.
Factory default value is 3.

13 Fan speed min

Minimal fan speed. The microcontroller sends out an interrupt request (if enabled) if the actual fan speed drops below this value. The default value is 0 RPM.

14 Fan speed max

Maximal fan speed. The microcontroller sends out an interrupt request (if enabled) if the actual fan speed exceeds this value. The default value is 30600 RPM.

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INTERRUPTS

15 High active

The microcontroller sends out a high active interrupt request (if enabled) if the temperature or the fan speed is out of the specified range.

16 Low active

The microcontroller sends out a low active interrupt request (if enabled) if the temperature or the fan speed is out of the specified range. Default value is IRQ low active.

17 IRQ on

Enables the interrupt requests sent out by the microcontroller if the temperature or the fan speed is out of the specified range.

18 IRQ off

Disables the interrupt requests sent out by the microcontroller if the temperature or the fan speed is out of the specified range. Default value is IRQ off.

19 IRQ5

The microcontroller sends out interrupt request 5 (if enabled) if the temperature or the fan speed is out of the specified range. IRQ10 and IRQ15 are disabled.

20 IRQ10

The microcontroller sends out interrupt request 10 (if enabled) if the temperature or the fan speed is out of the specified range. IRQ5 and IRQ15 are disabled.

21 IRQ15

The microcontroller sends out interrupt request 15 (if enabled) if the temperature or the fan speed is out of the specific range. IRQ5 and IRQ10 are disabled. Default value is IRQ15.

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OTHER PARAMETERS

22 Delay before PWRGD

Delay between the time when all voltages have got valid values and no manual reset is asserted and the rebooting of the PROFIVE CPU. If the microcontroller resets the PROFIVE CPU because one or more voltages are out of their specific ranges and then all voltages are in their specific ranges again or the manual reset is asserted and then the manual reset is cleared again this value specifies the delay before the PROFIVE CPU will reboot the system. Default value is 100 ms.

23 Delay before PWRGD at start

Delay between the time when all voltages have got valid values and no manual reset is asserted and the booting of the PROFIVE CPU after you have turned on the power supply of the PROFIVE CPU. Default value is 0 ms.

24 Manual reset delay

Delay between the assertion of the manual reset and the time when the microcontroller resets the PROFIVE CPU. Default value is 500 ms.

25 Time to ext. SOFTWARE watchdog timer (WDT) reset

Time within external software watchdog timer flag has to be cleared by software. If this flag is not cleared during this time the microcontroller resets the PROFIVE CPU. Default value is 25.5 s (25500 ms). For details see chapter „External Software Watchdog Timer“.

26 Delay before PWRGD after ext. SOFTWARE WDT reset

Delay time between resetting the PROFIVE CPU by microcontroller because external software WDT flag has been cleared and the time when the PROFIVE CPU will reboot the system. Default value is 100 ms. For details see chapter „External Software Watchdog Timer“.

27 Time to ext. HARDWARE watchdog timer (WDT) reset

Time in which external hardware watchdog timer flag has to be cleared by hardware. If this flag is not cleared during this time the microcontroller resets the PROFIVE CPU. Default value is 25.5 s (25500 ms). For details see chapter „External Hardware Watchdog Timer“.

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28 Delay before PWRGD after ext. HARDWARE WDT reset

Delay time between resetting the PROFIVE CPU by microcontroller because external hardware WDT flag has been cleared and the time when the PROFIVE CPU will reboot the system. Default value is 25.5 s (25500 ms). For details see chapter „External Hardware Watchdog Timer“.

29 Clear status byte

The status byte set by the microcontroller is cleared. This byte gives information about a failed I²C-bus transaction and about the source of interrupt request sended out by the microcontroller (temperature IRQ or fan IRQ).

30 Write to EEPROM

Writes a data byte to a specific address of the EEPROM.

31 Read from EEPROM

Reads a data byte from a specific address of the EEPROM.

0 NOTHING

No parameter is to be changed.

Remark:

The new values are stored in the EEPROM of the PROFIVE CPU-T5.

Some values are converted before storing in the EEPROM. If you type <r> after you have modified some parameter the actual values of the modified parameter can be different from the value you have entered before. This is the result of converting the new parameter twice. First before storing in the EEPROM and second when the values are read from the EEPROM and displayed on the screen.

To load the microcontroller default configuration, the UC_DEF_CFG pin must be pulled to GND during startup. For location of the UC_DEF_CFG pin see Appendix.

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7.2 CONF_ROM.EXE

The CONF_ROM.EXE is the program to configure the EEPROM of the PROFIVE CPU-T5. With this program you have the ability to configure the whole EEPROM (256 byte) loading a binary file in the EEPROM.

First copy the CONF_ROM.EXE file to your hard disk.

After you have installed the EXE-file you can execute the program to configure the EEPROM.

Syntax:

CONF_ROM [Option]

Option:

x.x Name of the binary file you want to load in the EEPROM

/? Information
Displays a short information on the screen

If you type CONF_ROM /? you will get the following short information on the screen:

```
------------------------------------------------------------------------
EEPROM Configuration of PROFIVE CPU-Series
Program CONF_ROM, Version x.x

PC/104-Plus PROFIVE CPU-Series Card by E.E.P.D.GmbH, Germany

Copyright (C) 1998 - 2000 by E.E.P.D. GmbH.
All rights reserved.
------------------------------------------------------------------------
Program to load a binary file into EEPROM (size: 256 byte).

SYNTAX: conf_rom x            x: Name of the binary file or
                                 /? Short information
------------------------------------------------------------------------
Address:

E.E.P.D. Electronic Equipment Produktion & Distribution GmbH
Gewerbering 3
D-85258 Weichs, Germany
Tel.: ++49-8136-9328-0
Fax.: ++49-8136-6910
Internet: http://www.eepd.com
------------------------------------------------------------------------
```


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If you type CONF_ROM x.x the program is executed. Then you will get the following message in DOS:

```
Find PCI-Device...passed
Find Base-Address...passed
Configure SMBus...done
Open Base-File...done

Write configuration to EEPROM of PROFIVE CPU-Series

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All rights reserved.
```

After the program is finished successfully the binary file has been loaded into the EEPROM.

Remark:

When you load the binary file CONFIG1.BIN into the EEPROM you get the default configuration of the PROFIVE CPU-T5 (same effect as pulling UC_DEF_CFG pin to GND during startup; for location of UC_DEF_CFG pin see Appendix).

When loading the binary file FACTTIL1.BIN into the EEPROM you get the factory default configuration of the PROFIVE CPU-T5.

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7.3 WDT_DEMO.EXE

The WDT_DEMO.EXE is a demo software which shows you how to handle the external software watchdog timer and the external hardware watchdog timer.

There is an excerpt of the source code of this demo software in Appendix **„Source Code of Demo Software WDT_DEMO.C“**.

With this excerpt you can develop your own application using the external software watchdog timer or the external hardware watchdog timer.

First copy the WDT_DEMO.EXE file to your hard disk.

After you have installed the EXE-file you can execute the program to handle the external software or hardware watchdog timer.

Syntax:

WDT_DEMO [Option]

Option:

swdton	x	Software WDT is enabled with parameter loaded from the EEPROM
	x:	Software watchdog timer flag in microcontroller is cleared every x * 100 ms by this software
swdtoff		Software WDT is disabled
hwdton		Hardware WDT is enabled with parameter loaded from the EEPROM
hwdtoff		Hardware WDT is disabled
s_hwdton	x	Soft- and hardware WDT are enabled with parameters loaded from EEPROM
	x:	Software watchdog timer flag in microcontroller is cleared every x * 100 ms by this software
s_hwdtoff		Soft- and hardware WDT are disabled
/?		Information Displays a short information on the screen

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```
If you type WDT_DEMO /? you will get following short information on the screen:
-------------------------------------------------------------------------
Demo Software for External Software and Hardware Watchdog Timer
of PROFIVE CPU-Series

This software is a demo software which shows how to handle the
external software and hardware watchdog timer of the
PROFIVE CPU-Series card.The demo software activates
external software and/or hardware watchdog timer and clears
the external watchdog timer flag in the microcontroller
every x*100 milliseconds. If you quit the demo software the
external software watchdog timer will be deactivated (If you
have called WDT_SW01.EXE without parameters!)

The POWER MANAGEMENT has to be DISABLED!

Microcontroller Program Version xx

Program WDT_DEMO, Version x.x

-------------------------------------------------------------------------
Type <ENTER>.....!
```

After typing <ENTER> following information appears:

```
-------------------------------------------------------------------------
SYNTAX: wdt_demo  swdton   x  Software WDT on with parameter loaded
                               from EEPROM
                               x: Reset time of external software WDT flag
                                  Reset time = x*100 ms
        wdt_demo  swdtoff     Software wdt off
        wdt_demo  hwdton      Hardware wdt on with parameter loaded
                               from EEPROM
        wdt_demo  hwdtoff     Hardware wdt off
        wdt_demo  s_hwdton x  Soft- and hardware wdt on with parameter
                               loaded from EEPROM
                               x: Reset time of external software WDT flag
                                  Reset time = x*100 ms
        wdt_demo  s_hwdtoff   Soft- and hardware wdt off

PC/104-Plus PROFIVE CPU-Series Card by E.E.P.D. GmbH, Germany

Copyright (C) 1998 by E.E.P.D. GmbH. All rights reserved.
-------------------------------------------------------------------------
Address:
E.E.P.D. Electronic Equipment Produktion & Distribution GmbH
Gewerbering 3
D-85258 Weichs, Germany
Tel.: ++49-8136-9328-0
Fax.: ++49-8136-6910
Internet: http://www.eepd.com
-------------------------------------------------------------------------

Type <ENTER> to quit program help!
```


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If you type WDT_DEMO without an option the program is executed menu driven. Then you will get following message in DOS:

```
Demo-Software for External Software and Hardware Watchdog Timer
of PROFIVE CPU-Series!

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All rights reserved.

Activate Software <s> or Hardware <h> Watchdog Timer:
```

External Software WDT

If you type <s> the parameters of the external software watchdog timer appear on the display:

```
Time for ext. software watchdog timer (WDT) reset  x ms
Delay before PWRGD after ext. software WDT reset   x ms

Reset ext. software watchdog timer flag after x*100 milliseconds:
```

Now you have to set the parameter of the reset time of software WDT flag. After this time the software watchdog timer flag in the microcontroller is cleared by this software.

When the parameter of the reset time of software WDT flag is correct (in the range of 0..255) you will see all parameter of the external software WDT again:

```
      PARAMETER OF EXTERNAL SOFTWARE WATCHDOG TIMER

Time for ext. software watchdog timer (WDT) reset  x ms
Delay before PWRGD after ext. software WDT reset   x ms
Reset ext. software watchdog timer flag after      x ms

Do you want to activate the external software watchdog timer
with this parameters: <y>, <n>
```

Type <y> if you want to activate the external software WDT. The following message appears on the screen:

```
External software watchdog timer is activated!
Press key to deactivate external software watchdog timer.
```

The external software watchdog timer is activated now until a key is pressed.

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External Hardware WDT

If you type <h> at the beginning of the demo program you will activate the external hardware watchdog timer. The following message appears on the screen:

```
External hardware watchdog timer is activated!
Reboot PC or call 'wdt_demo hwdtoff' to deactivate external
hardware watchdog timer.
```

The external hardware watchdog timer is activated now until you call „WDT_DEMO hwdtoff“ or the PROFIVE CPU is rebooted.

Make sure that you have sent out the signal to EXT_WD_INP pin which clears the hardware watchdog timer flag in the microcontroller first. For location of EXT_WD_INP pin see Appendix.

For details of the external software watchdog timer and the external hardware watchdog timer see chapter „External Software Watchdog Timer“ or chapter „External Hardware Watchdog Timer“ respectively.

7.3.1 External Software Watchdog Timer

The external software watchdog timer (WDT) is a method to control the activity of the system by software. The handling of the external software WDT is shown in the demo software WDT_DEMO.EXE. If the external software WDT is enabled a software watchdog timer flag has to be cleared by software within x ms. Clearing of this flag has to be done via I²C-Bus. The time x is called „Time to ext. SOFTWARE watchdog timer (WDT) reset“ and can be configured with the program CONF_P5.EXE. The microcontroller resets the PROFIVE CPU if the software WDT flag is not cleared within the time x. After reset the PROFIVE CPU will reboot after delay time y which is called „Delay before PWRGD after ext. SOFTWARE WDT reset“. The external software WDT is always disabled after reboot.

The I²C-Bus master device is the Intel PIIX4 chipset. All transactions on the I²C-Bus are done via this I²C-Bus master device.

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For the external software watchdog timer the following commands on the I²C-Bus are available:

- Clear software watchdog timer flag in the microcontroller

Write Data Byte **0x25** via I²C-Bus to the microcontroller,
microcontroller has got I²C-Bus 7 bit slave address 1000100

I²C-Bus Protocol:

S	Slave Address (1000100)	Wr (0)	A	Data Byte **(0x25)**	A	P

- Enable software watchdog timer in the microcontroller

Write Data Byte **0x26** via I²C-Bus to the microcontroller,
microcontroller has got I²C-Bus 7 bit slave address 1000100

I²C-Bus Protocol:

S	Slave Address (1000100)	Wr (0)	A	Data Byte **(0x26)**	A	P

- Disable software watchdog timer in the microcontroller

Write Data Byte **0x27** via I²C-Bus to the microcontroller,
microcontroller has got I²C-Bus 7 bit slave address 1000100

I²C-Bus Protocol:

S	Slave Address (1000100)	Wr (0)	A	Data Byte **(0x27)**	A	P

S: Start Condition
P: Stop Condition
A: Acknowledge
Wr: Write

☐ Master to Slave (PIIX4 is master, microcontroller is slave)

☐ Slave to Master (PIIX4 is master, microcontroller is slave)

Remark:

The external software watchdog timer will only work correctly if the POWER MANAGEMENT is DISABLED in the system bios.

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7.3.2 External Hardware WatchdogTimer

The external hardware watchdog timer (WDT) is a method to control the activity of the system by hardware. The handling of the external hardware WDT is shown in the demo software WDT_DEMO.EXE. If the external hardware WDT is enabled a hardware watchdog timer flag has to be cleared by hardware within x ms. Therefor at least one pulse with a minimal pulse width of 520 ns has to be sent out to the EXT_WD_INP pin (for location of EXT_WD_INP pin see Appendix). The time x is called „Time to ext. HARDWARE watchdog timer (WDT) reset“ and can be configured with the program CONF_P5.EXE. The microcontroller resets the PROFIVE CPU if the hardware WDT flag is not cleared within the time x. After reset the PROFIVE CPU will reboot the system after delay time y which is called „Delay before PWRGD after ext. HARDWARE WDT reset“. The external hardware WDT is always disabled after reboot.

For the external hardware watchdog timer following commands on the I²C-Bus are possible:

- Enable hardware watchdog timer in the microcontroller

Write Data Byte **0x23** via I²C-Bus to the microcontroller,
microcontroller has got I²C-Bus 7 bit slave address 1000100

I²C-Bus Protocol:

S	Slave Address (1000100)	Wr (0)	A	Data Byte **(0x23)**	A	P

- Disable hardware watchdog timer in the microcontroller

Write Data Byte **0x24** via I²C-Bus to the microcontroller,
microcontroller has got I²C-Bus 7 bit slave address 1000100

I²C-Bus Protocol:

S	Slave Address (1000100)	Wr (0)	A	Data Byte **(0x24)**	A	P

S: Start Condition
P: Stop Condition
A: Acknowledge
Wr: Write

☐ Master to Slave (PIIX4 is master, microcontroller is slave)

▒ Slave to Master (PIIX4 is master, microcontroller is slave)

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7.4 Access to the I²C-Bus

The access to the I²C-Bus happens through the Intel PIIX4 chipset as I²C-Bus master device. Communication between the I²C-Bus master and following slave devices is possible:

Slave Device	7 bit Slave Address
Microcontroller	1000100
EEPROM	1010100
Digital Temperature Sensor	1001001

7.4.1 Read Values from EEPROM

I²C-Bus Protocol:

S	Slave Address (1010100)	Wr (0)	A	Address Byte	A	S	Slave Address (1010100)	Rd (1)	A	Data Byte	A	P

The Address Byte is the address of the data in the EEPROM that want to be read. The Data Byte is the return value sent from the EEPROM to the master device. See chapter „Address Mapping of EEPROM“.

7.4.2 Write Values to EEPROM

I²C-Bus Protocol:

S	Slave Address (1010100)	Wr (0)	A	Address Byte	A	Data Byte	A	P

The Address Byte is the address of the data in the EEPROM that want to be written with the value of Data Byte. See chapter „Address Mapping of EEPROM“.

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7.4.3 Read Values from Digital Temperature Sensor

I²C-Bus Protocol:

S	Slave Address (1001001)	Wr (0)	A	Address Byte	A	S	Slave Address (1001001)	Rd (1)	A	Data Byte High	A	Data Byte Low	A	P

The Address Byte is the Pointer Byte of the digital temperature sensor. Data Byte High and Data Byte Low are the return values sent from the digital temperature sensor to the master device.

Pointer Byte	Function
0x00	actual temperature (read only)
0x02	maximal temperature (read – write)
0x03	hysterese temperature (read – write)

The temperature registers have following structure:

Data Byte High								Data Byte Low							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB	x	x	x	x	x	x	x

One LSB = 0.5 °C, two's complement format.

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7.4.4 Write Values to Digital Temperature Sensor

I²C-Bus Protocol:

S	Slave Address (1001001)	Wr (0)	A	Address Byte	A	Data Byte High	A	Data Byte Low	A	P

The Address Byte is the Pointer Byte of the digital temperature sensor. Data Byte High and Data Byte Low are the values that want to be written.

Pointer Byte	Function
0x02	maximal temperature (read – write)
0x03	hysterese temperature (read – write)

The temperature registers have following structure:

Data Byte High								Data Byte Low							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB	x	x	x	x	x	x	x

One LSB = 0.5 °C, two's complement format.

7.4.5 Read Values from Microcontroller

I²C-Bus Protocol:

S	Slave Address (1000100)	Wr (0)	A	Address Byte	A	S	Slave Address (1000100)	Rd (1)	A	Data Byte	A	P

The Address Byte is the Command Byte of the microcontroller. The Data Byte is the return value sent from the microcontroller to the master device.

Command Byte	Function
0xF0	Read actual voltage of CPUVCORE
0xF1	Read actual voltage of CPUVIO
0xF2	Read actual voltage of P3V3
0xF3	Read actual voltage of VCC_MESS
0xF4	Read actual fan speed
0xF5	Read status byte

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7.4.6 Write Values to Microcontroller

I²C-Bus Protocol:

S	Slave Address (1000100)	Wr (0)	A	Data Byte	A	P

The Data Byte is the Command Byte sent to the microcontroller.

Command Byte	Function
0x22	Clear status byte
0x23	Enable hardware watchdog timer
0x24	Disable hardware watchdog timer
0x25	Clear software watchdog timer flag
0x26	Enable software watchdog timer
0x27	Disable software watchdog timer

S: Start Condition
P: Stop Condition
A: Acknowledge
A: No Acknowledge
Rd: Read
Wr: Write

☐ Master to Slave (PIIX4 is master, microcontroller is slave)

▒ Slave to Master (PIIX4 is master, microcontroller is slave)

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8 Support

Internet/eMail support

Internet: **http://www.eepd.com**
eMail: **support@eepd.com**

Please stop by to find new drivers and/or links to related webpages.

In order to process your request as fast as possible, we would need the following informations:

Complete address including phone and fax number
Delivery date
Product version
Type and serial-number of the product
Type of CPU used
Operating System used incl. version info
Type of memory module used
Setting of rotary switch
Configuration of Your System (all boards)
A short description of the problem

In the future there will be also a service request form available on our homepage http://www.eepd.com.

Voice/Fax support

Telephone: **++49-(0)8136-9328-0**
Fax: **++49-(0)8136-6910**

please skip (0) if dialing from outside of Germany

REMARK:

Prior notification by fax or via eMail is desired to avoid any misinterpretations and to accelerate response.

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9 Appendix

9.1 Address Mapping of Serial EEPROM

The EEPROM contains configuration information for the microcontroller of the PROFIVE CPU series

.

Address	Microcontroller Default	Factory Default	Description of Contents
00	00	54	CPUVCORE min
01	FF	80	CPUVCORE max
02	00	75	CPUVIO min
03	FF	A2	CPUVIO max
04	00	A8	P3V3 min
05	FF	D4	P3V3 max
06	00	C5	VCC_MESS min
07	FF	F1	VCC_MESS max
08	03	03	Using IRQ5 (1) / IRQ10 (2) / IRQ15 (3)
09	01	01	Delay before PWRGD
0A	05	05	Manual reset delay
0B	00	00	IRQ high (1) / low (0) active
0C	05	05	reserved, do not change!!
0D	01	03	Pulse per rotation of fan
0E	00	00	Fan speed min
0F	FF	FF	Fan speed max
10	80	80	reserved, do not change!!
11	78	78	Temperature max
12	6E	6E	Temperature hysterese
13	00	00	Delay before PWRGD at start
14	00	00	IRQ on(1)/off(0)
15	01	01	Delay before PWRGD after external software watchdog timer reset
16	FF	FF	Time for external software watchdog timer reset
17	01	01	Delay before PWRGD after external hardware watchdog timer reset
18	FF	FF	Time for external hardware watchdog timer reset
FD	00	00	Temperature in °C(0) or °F(1)
FE	xx	xx	Revision of microcontroller program, do not change!!
FF	5A	5A	reserved, do not change!!

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9.2 Source Code of Demo Software WDT_DEMO.C

This appendix is an excerpt of the source code of demo software WDT_DEMO.EXE which shows how to handle the external software watchdog timer and the external hardware watchdog timer.

With this excerpt you can develop your own application using one of these watchdog timers.

```
/*****************************************************************************/
/*                                                                           */
/* This program is the confidential and proprietary product of E.E.P.D. GmbH.*/
/* Any unauthorized use, reproduction or transfer of this program is strictly prohibited. */
/* Copyright (c) 1999 by E.E.P.D. GmbH. All rights reserved.                 */
/*                                                                           */
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/*                                                                           */
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/* E.E.P.D.'s products are not intended for use as critical components in life support   */
/* appliances, devices or systems in which the failure of a E.E.P.D. product to perform  */
/* could be expected to result in personal injury.                           */
/* All mentioned trademarks are registered trademarks of their owner.        */
/*                                                                           */
/* Description: EXCERPT of source code of the demo software WDT_DEMO.EXE     */
/*              for PROFIVE CPU-Series Card                                  */
/*                                                                           */
/*              This is an EXCERPT of the source code of the demo software WDT_DEMO.EXE  */
/*              which shows how to handle the external software and hardware watchdog    */
/*              timer of the PROFIVE CPU-Series card.                        */
/*              The demo software activates the external SW watchdog timer and clears the */
/*              external watchdog timer flag in the microcontroller every x milliseconds. */
/*              If you quit the demo software the external watchdog timer will be        */
/*              deactivated.                                                 */
/*              Further on the external hardware watchdog timer can be activated and     */
/*              deactivated.                                                 */
/*              The POWER MANAGEMENT has to be DISABLED for ext. SOFTWARE WDT!           */
/*              Copyright (C) 1999 by E.E.P.D. GmbH.                         */
/*              All rights reserved.                                         */
/*                                                                           */
/* Address:     E.E.P.D. Electronic Equipment Produktion & Distribution GmbH             */
/*              Gewerbering 3                                                */
/*              D-85258 Weichs, Germany                                      */
/*              Tel.: ++49-8136-9328-0                                       */
/*              Fax.: ++49-8136-6910                                         */
/*              Internet: http://www.eepd.com                                */
/*                                                                           */
/* Compiler:    WATCOM                                                       */
/* Developer:   Dipl.-Ing. Thomas Vahle, E.E.P.D. GmbH                       */
/* Date:        04.08.1999                                                   */
/* Last Update: 05.11.1999                                                   */
/*                                                                           */
/*****************************************************************************/

#include <...>                          // add necessary include-files

const unsigned int   eepromr = 0xa9,    // slave address of eeprom for read from eeprom
```


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```
                    uc_picw = 0x88;   // slave address of microcontroller for write
                                      // to this device

int    ext_wdt_out_s,              // value in EEPROM, delay before PWRGD after SW WDT RESET
       ext_wdt_time_s,             // value in EEPROM, time for external SW WDT RESET
       rev;                        // value in EEPROM, revision of microcontroller firmware

unsigned int  base,                // SMBus base address (PIIX4 is SMBus Master device)
              addr,                // address variable
              bus_nr,              // Bus Number
              dev,                 // Device and Function Number
              SMBHSTDAT0,          // PIIX4 SMB-register SMBHSTDAT0 variable
              SMBHSTSTS;           // PIIX4 SMB-register SMBHSTSTS  variable

.
.
.

//*********************************************************************************************
// Find PCI device

void find_device ()
  {
   .
   .
   .
   // PCI_FUNCTION: FIND_PCI_DEVICE                (AL): 0x02
   // PCI_FUNCTION_ID                              (AH): 0xB1
   // Device ID of Intel PIIX4 (SMB Master device) (CX): 0x7113
   // Vendor ID of Intel PIIX4 (SMB Master device) (DX): 0x8086
   // Index(0...N)                                 (SI): 0x00
   // Interrupt: INT 0x1A
   //
   // RETURN VALUES: Bus Number                    (BH)
   //                Device and Function Number    (BL)
   //
   // For details refer to the "PCI BIOS SPECIFICATION Revision 2.1, August 26, 1994"
   .
   .
   .
  }

//*********************************************************************************************
// Find SMBus base address (PIIX4 is SMB Master device)

void find_base_addr ()
  {
   .
   .
   .
   // PCI_FUNCTION: READ_CONFIG_WORD                              (AL): 0x09
   // PCI_FUNCTION_ID                                             (AH): 0xB1
   // Register Number (0,2,4,...,254)                             (DI): 0x90
   // Bus Number (0...255), return value of FIND_PCI_DEVICE       (BH)
   // Device and Function Number, return value of FIND_PCI_DEVICE (BL)
   // Interrupt: INT 0x1A
   //
   // RETURN VALUE: Word Read                                     (CX): base
   //
   // For details refer to the "PCI BIOS SPECIFICATION Revision 2.1, August 26, 1994"
   .
   .
   .
  }

//*********************************************************************************************
// Configure PIIX4 for SMBus access

void smb_config ()
```


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```
  {
   .
   .
   .
   // PCI_FUNCTION: WRITE_CONFIG_BYTE                              (AL): 0x0B
   // PCI_FUNCTION_ID                                              (AH): 0xB1
   // Register Number (0,2,4,...,254)                              (DI): 0xD2
   // Byte value to write                                          (CL): 0x01
   // Bus Number (0...255), return value of FIND_PCI_DEVICE        (BH)
   // Device and Function Number, return value of FIND_PCI_DEVICE  (BL)
   // Interrupt: INT 0x1A
   //
   // For details refer to the "PCI BIOS SPECIFICATION Revision 2.1, August 26, 1994"
   .
   .
   .
  }

//*****************************************************************************************
// Check if IIC-Bus is busy until bus is free

void iic_busy()
  {
   int  ssp_busy;

   SMBHSTSTS = inp(base);          // read contents of PIIX4 SMB-register SMBHSTSTS
   ssp_busy = SMBHSTSTS & 0x01;
   while (ssp_busy)                // check IIC-Bus until bus is free
        {
         SMBHSTSTS = inp(base);
         ssp_busy = SMBHSTSTS & 0x01;
        }
  }

//*****************************************************************************************
// Read byte from IIC device via IIC-Bus

void reg_read (unsigned int dev_addr, unsigned int reg_addr)
  {
   unsigned int in, addr;

   addr = base + 0x04;
   in = outp(addr,dev_addr);       // device address, read
   addr = base + 0x03;
   in = outp(addr,reg_addr);       // address in device, command byte
   addr = base + 0x05;
   in = outp(addr, 0x00);          // data0 register is reset
   addr = base;
   in = outp(addr,0x1e);
   addr = base + 0x02;
   in = outp(addr,0x48);          // start execution, interrupt disable, set HOST CTRL REG
  }

//*****************************************************************************************
// Write byte to microcontroller via IIC-Bus

void reg_write_pic (unsigned int dev_addr, unsigned int b1)
  {
   unsigned int in, addr;

   addr = base + 0x04;
   in = outp(addr, dev_addr);      // device address, write
   addr = base + 0x03;
   in = outp(addr, b1);            // First Byte , command byte
   addr = base + 0x05;
   in = outp(addr, 0x00);          // Second Byte
   addr = base;
   in = outp(addr,0x1e);
   addr = base + 0x02;
```


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```
    in = outp(addr,0x44);           // start execution, interrupt disable, set HOST CTRL REG
  }

//*****************************************************************************************
// wait for n*100 ms, delay function for external software watchdog timer

void wait (int n)
  {
   .
   .
   .
   // place delay function for external software watchdog timer
   // delay function should cause an delay of n*100 ms
   .
   .
   .
  }

//*****************************************************************************************
// Main program

void main()
  {

   int ext_wdt_reset;              // after this time the external watchdog timer flag
                                   // is cleared (ext_wdt_reset * 100 ms)

// *****************************************************************************************
// find device, find SMBus base address and configure SMBus

   find_device();
   find_base_addr();
   smb_config();

// *****************************************************************************************
// read revision of microcontroller firmware

   iic_busy();
   reg_read(eepromr,0xfe);         // read revision of microcontroller firmware
   wait(1);                        // wait for 100 ms
   addr = base + 0x05;
   rev = inp(addr);                // external software watchdog timer and external hardware
                                   // watchdog timer is only available for rev >= 0x2A

// *****************************************************************************************
// Initialization of external software WDT, external software WDT is activated

   iic_busy();
   reg_write_pic(uc_picw,0x25);    // external SW WDT Flag is set to 0
   wait(1);
   iic_busy();
   reg_write_pic(uc_picw,0x26);    // external SW WDT is activated


// *****************************************************************************************
// Loop which resets the external SW WDT Flag

   while (!kbhit())
        {
         wait(ext_wdt_reset);      // wait for ext_wdt_reset * 100 ms
                                   // Reset ext. software watchdog timer flag after
                                   // ext_wdt_reset * 100 milliseconds
                                   // 0 < ext_wdt_reset < 256
         iic_busy();
         reg_write_pic(uc_picw,0x25);      // external SW WDT Flag in uC is set to 0
        }

// *****************************************************************************************
// External SW WDT is deactivated
```


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```
   iic_busy();
   reg_write_pic(uc_picw,0x27);     // external SW WDT is deactivated

   .
   .
   .


// ********************************************************************************
// External HW WDT is activated

   iic_busy();
   reg_write_pic(uc_picw,0x23);     // external HW WDT is activated

   .
   .
   .


  }                                 //  end of main program
```


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9.3 Starter-Kit

To get started easily a starter-kit is available for the CPU-T5. The starter-kit for the PROFIVE CPU-T5 is containing all cables and adaptation boards needed to connect standard devices to the PROFIVE CPU-T5V. Following components are included in the starter kit of the PROFIVE CPU-T5:

- 4 x cable for RS 232 serial port
- 1 x cable for 1*2.5" IDE
- 1 x adaptation board for floppy drive, incl. FFC cable/1.00 pitch
- 1 x cable for power supply
- 1 x adaptation board for keyboard, mouse and USB, incl. cables
- 1 x adaptation board for LPT port, incl. FFC cable/1.00 pitch
- 1 x bag with mounting screws, nuts and bolts

9.4 DC Drive Capability

Description	Connector	DC Current	fused
USB_VCC	X4.6	1.0 A	•
SPKR_VCC	X4.9	0.3 A	•
P5V_SAFE	Reserved for IR application	(0.3 A)	•
PS/2_MS_VCC	X17.2	0.3 A	•
KEYB_VCC	X17.6	0.3 A	•
FDDVCC	X6.3, X6.3, X6.5	1.0 A (together)	•
VCC PC104 Bus (ISA)	X8/B.3, X8/B.29, X9/D.16	1.0 A (each Pin)	
VCC PC 104-plus Bus (PCI)	X14A.22, X14A.26, X14B.21, X14B.27, X14C.1, X14C.24, X14C.28, X14D.2	1.0 A (each Pin)	

Caution!

Maximum DC input current at X5 (terminal screw) may not exceed 8.0 Amperes

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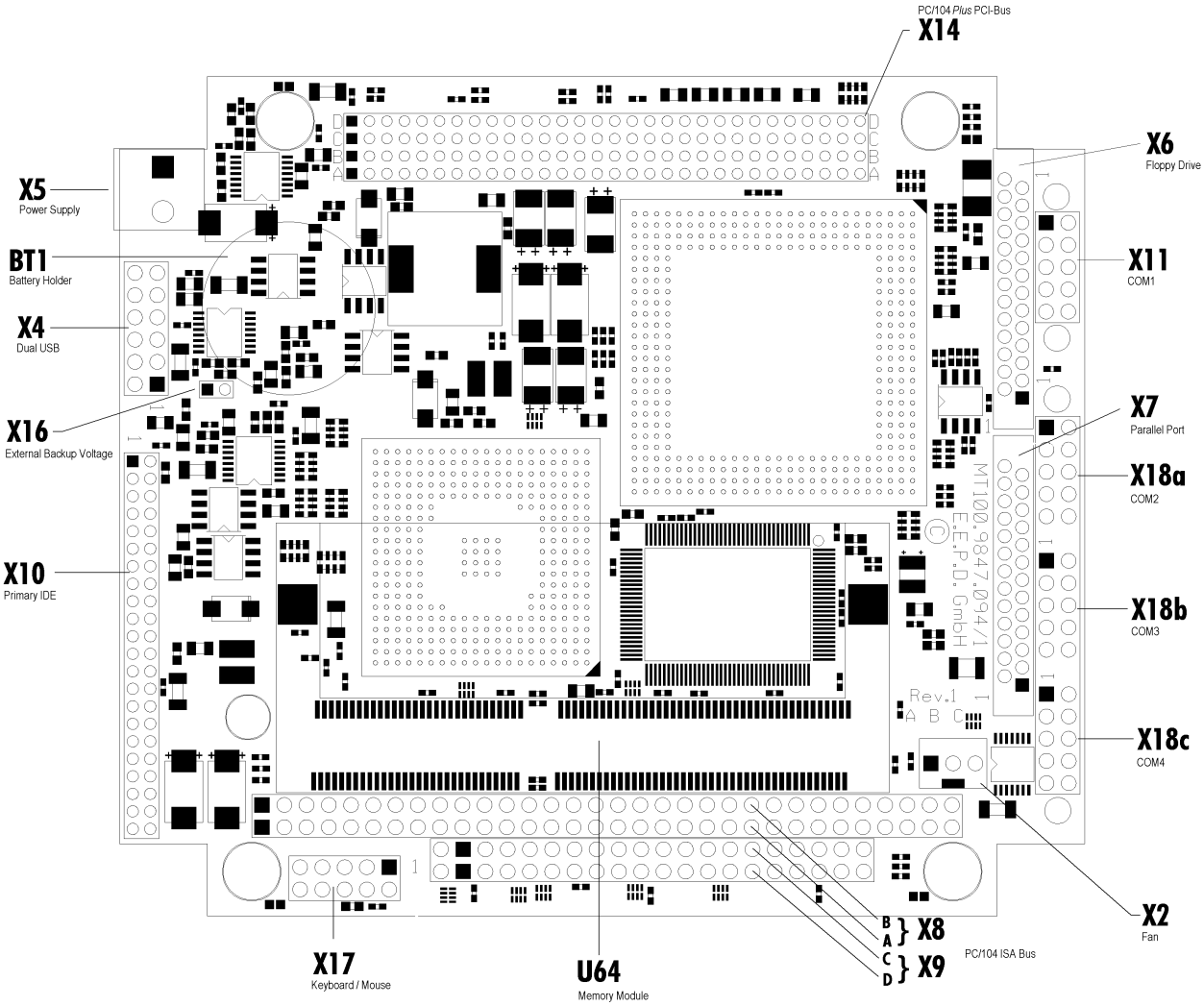
9.5 Connector Description

9.5.1 Connector Location



Layout diagram: component side

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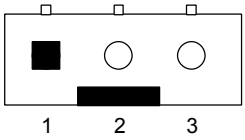
9.5.2 Connector Pinout Description

NOTE: All signals followed by " - " are active low signals.

9.5.2.1 X2 Fan Connector (optional)

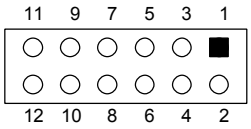
Pin	Description	Pin	Description
1	VCC (+5V)	2	FAN_SPEED
3	GND		



X2 fan connector

9.5.2.2 X4 Universal Serial Bus

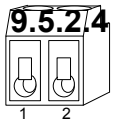
Pin	Description	Pin	Description
1	EXT_WD_INP	2	UC_DEF_CFG-
3	HDD_LED (-)	4	HDD_LED (+)
5	USBP0-P	6	USB_VCC
7	USBP0-M	8	USB_GND
9	SPKR_VCC	10	SPKR_GND
11	USBP1-P	12	USBP1-M



X4 dual USB connector

9.5.2.3 X5 Power Supply

Pin	Description	Pin	Description
1	GND	2	VCC



X5 power supply

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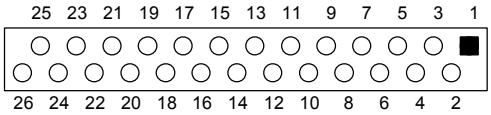
X6 Floppy Connector

Pin	Description	Pin	Description
1	VCC	14	STEP-
2	INDEX-	15	GND
3	VCC	16	WDATA-
4	DRIVESEL0-	17	GND
5	VCC	18	WGATE-
6	DISKCHANGE-	19	GND
7	NC	20	TRACK0-
8	NC	21	GND
9	DRVDEN0	22	WRITE_PROT-
10	MOTOR0-	23	GND
11	NC	24	READ_DATA-
12	DIRECTION-	25	GND
13	NC	26	HEAD_SEL-

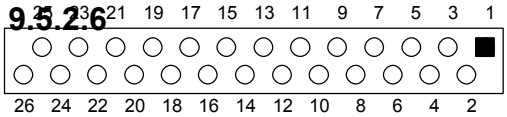


X6 floppy connector

9.5.2.5 X7 Parallel Port

Pin	Description	Pin	Description
1	STROBE-	14	SLIN-
2	PDATA0	15	INIT-
3	PDATA1	16	ERR-
4	PDATA2	17	AFD-
5	PDATA3	18	GND
6	PDATA4	19	GND
7	PDATA5	20	GND
8	PDATA6	21	GND
9	PDATA7	22	GND
10	ACK-	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT	26	GND

9.5.2.6



X7 parallel port

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X8/X9 PC/104-*Plus* ISA-Bus Connector

Pin	X8/A	X8/B	X9/C	X9/D
0			GND	GND
1	IOCHCHK-	GND	SBHE-	MEMCS16-
2	SD7	RESETDRV	LA23	IOCS16-
3	SD6	VCC	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	NC(M5V)	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	NC(M12V)	LA18	IRQ14
8	SD1	0WS-	LA17	DACK0-
9	SD0	N.C. (P12V)	MEMR-	DRQ0
10	IOCHRDY-	KEY	MEMW-	DACK5-
11	AEN	SMEMW-	SD8	DRQ5
12	SA19	SMEMR-	SD9	DACK6-
13	SA18	IOW-	SD10	DRQ6
14	SA17	IOR-	SD11	DACK7-
15	SA16	DACK3-	SD12	DRQ7
16	SA15	DRQ3	SD13	VCC
17	SA14	DACK1-	SD14	MASTER-
18	SA13	DRQ1	SD15	GND
19	SA12	REFRESH-	KEY	GND
20	SA11	SYSCLK		
21	SA10	IRQ7		
22	SA9	IRQ6		
23	SA8	IRQ5		
24	SA7	IRQ4		
25	SA6	IRQ3		
26	SA5	DACK2-		
27	SA4	TC		
28	SA3	BALE		
29	SA2	VCC		
30	SA1	OSC		
31	SA0	GND		
32	GND	GND		

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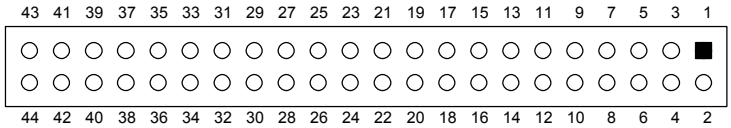
9.5.2.7 X10 IDE Connector

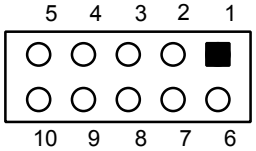
Pin	Description	Pin	Description
1	RESET_IDE	2	GND
3	DATA_07	4	DATA_08
5	DATA_06	6	DATA_09
7	DATA_05	8	DATA_10
9	DATA_04	10	DATA_11
11	DATA_03	12	DATA_12
13	DATA_02	14	DATA_13
15	DATA_01	16	DATA_14
17	DATA_00	18	DATA_15
19	GND	20	NC
21	IDE_DRQ	22	GND
23	IDE_IOW	24	GND
25	IDE_IOR	26	GND
27	IDE_IOCHRDY	28	IDE_SELA
29	IDE_ACK-	30	GND
31	IDE_IRQ	32	NC
33	HOST_A1	34	NC
35	HOST_A0	36	HOST_A2
37	IDE_CS0-	38	IDE_CS1-
39	HDD_ACT-	40	GND
41	VCC	42	VCC
43	GND	44	NC



X10 IDE connector

9.5.2.8 X11 COM1

Pin	Description	Pin	Description
1	DCD	6	DSR
2	RXD	7	RTS
3	TXD	8	CTS
4	DTR	9	RI
5	GND	10	NC



X11 COM1 connector

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9.5.2.9 X14 PC/104-*Plus* PCI-Bus Connector

Pin	X14A	X14B	X14C	X14D
1	GND	NC	VCC	AD0
2	VI_O(5V)	AD2	AD1	VCC
3	AD5	GND	AD4	AD3
4	C_BE0-	AD7	GND	AD6
5	GND	AD9	AD8	GND
6	AD11	VI_O(5V)	AD10	M66EN
7	AD14	AD13	GND	AD12
8	NC(P3V3)**	C_BE1-	AD15	NC(P3V3)**
9	SERR-	GND	SBO-	PAR
10	GND	PERR-	NC(P3V3)**	SDONE
11	STOP-	NC(P3V3)**	LOCK-	GND
12	NC(P3V3)**	TRDY-	GND	DEVSEL-
13	FRAME-	GND	IRDY-	NC(P3V3)**
14	GND	AD16	NC(P3V3)**	C_BE2-
15	AD18	NC(P3V3)**	AD17	GND
16	AD21	AD20	GND	AD19
17	NC(P3V3)**	AD23	AD22	NC(P3V3)
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C_BE3-	VI_O(5V)	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	VCC	AD28	AD27
22	VCC	AD30	GND	AD31
23	REQ0-	GND	REQ1-	VI_O(5V)
24	GND	REQ2-	VCC	GNT0-
25	GNT1-	VI_O(5V)	GNT2-	GND
26	VCC	PCLK0	GND	PCLK1
27	PCLK2	VCC	PCLK3	GND
28	GND	INTD	VCC	PCIRST-
29	NC(P12V)	INTA	INTB	INTC
30	NC(M12V)	NC	NC	GND

** contact factory if you need 3.3 V supplied on PC104-plus connector

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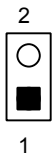
9.5.2.10 X16 External Backup Voltage Connector

Pin	Description	Pin	Description
1	GND	2	Vbat*

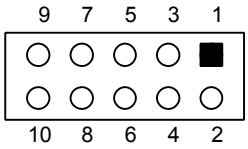


X16 external backup voltage connector

* typ. 3.0 V max 3.6 .

9.5.2.11 X17 Keyboard/Mouse Connector

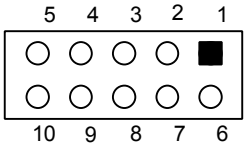
Pin	Description	Pin	Description
1	PS/2_MS_CLK	2	PS/2_MS_VCC
3	PS/2_MS_DATA	4	PS/2_MS_GND
5	KEYB_CLK	6	KEYB_VCC
7	KEYB_DATA	8	KEYB_GND
9	MAN_RESET-	10	GND



X17 keyboard/mouse connector

9.5.2.12 X18 a COM 2

Pin	Description	Pin	Description
1	DCD	6	DSR
2	RXD	7	RTS
3	TXD	8	CTS
4	DTR	9	RI
5	GND	10	NC



X18a COM2 connector

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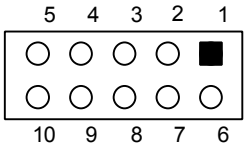
9.5.2.13 X18 b COM 3

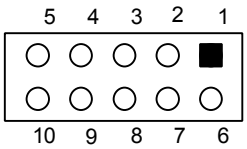
Pin	Description	Pin	Description
1	DCD	6	DSR
2	RXD	7	RTS
3	TXD	8	CTS
4	DTR	9	RI
5	GND	10	NC



X18b COM3 connector

9.5.2.14 X18 c COM 4

Pin	X18c	Pin	X18c
1	DCD	6	DSR
2	RXD	7	RTS
3	TXD	8	CTS
4	DTR	9	RI
5	GND	10	NC



X18c COM4 connector

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